Presentation Slides

Appendix B
Playing With NCL

Logically Determined Design:
Clockless System Design With NULL Convention Logic

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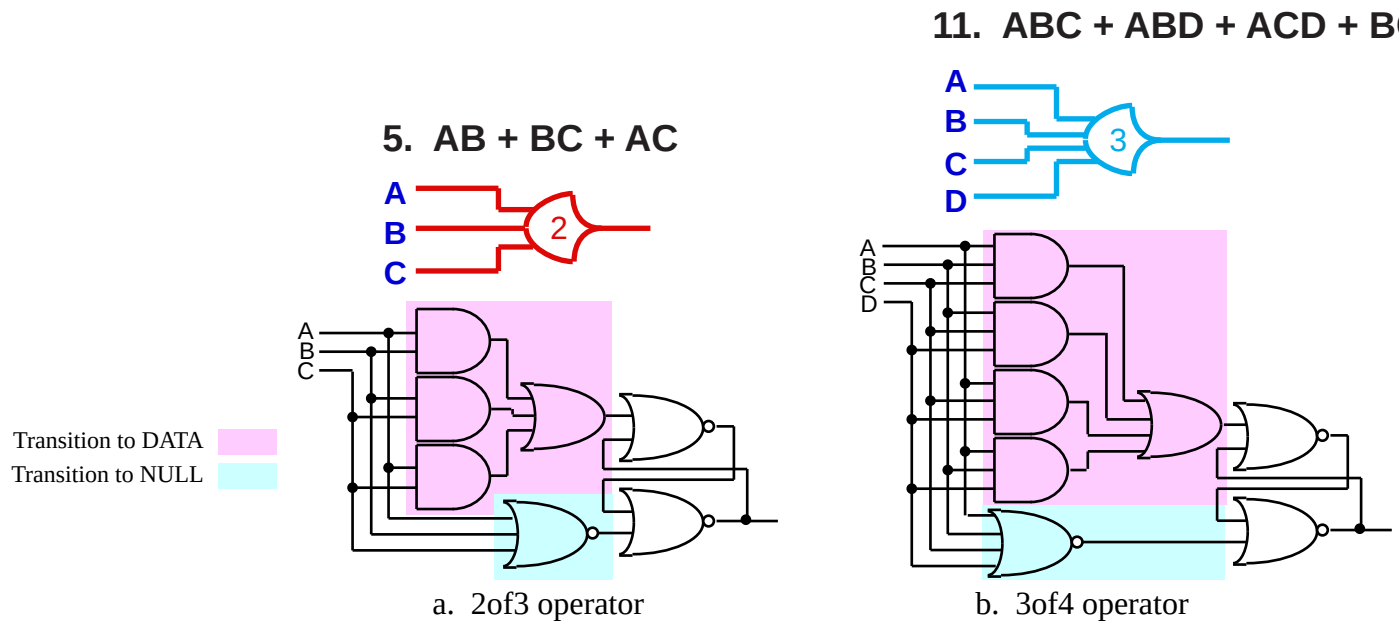
How to implement NCL in FPGAs

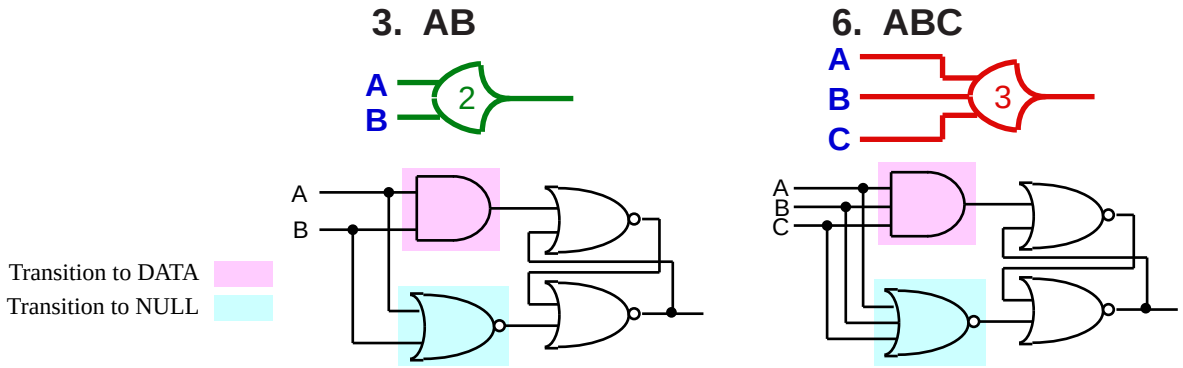
Method One

Map NCL gates to Boolean SR flip flop circuits
The resulting Boolean net list is mapped into the FPGA



a. 2of3 operator

b. 3of4 operator

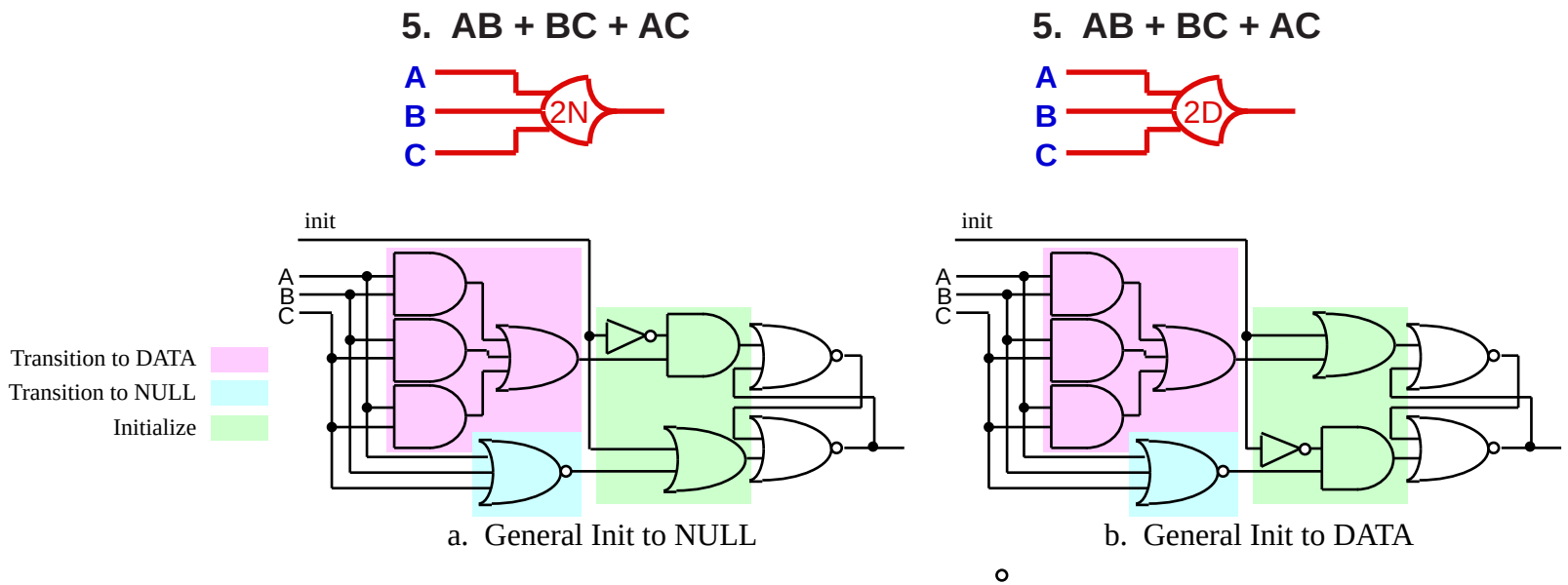


a. 2of2 operator

b. 3of3 operator

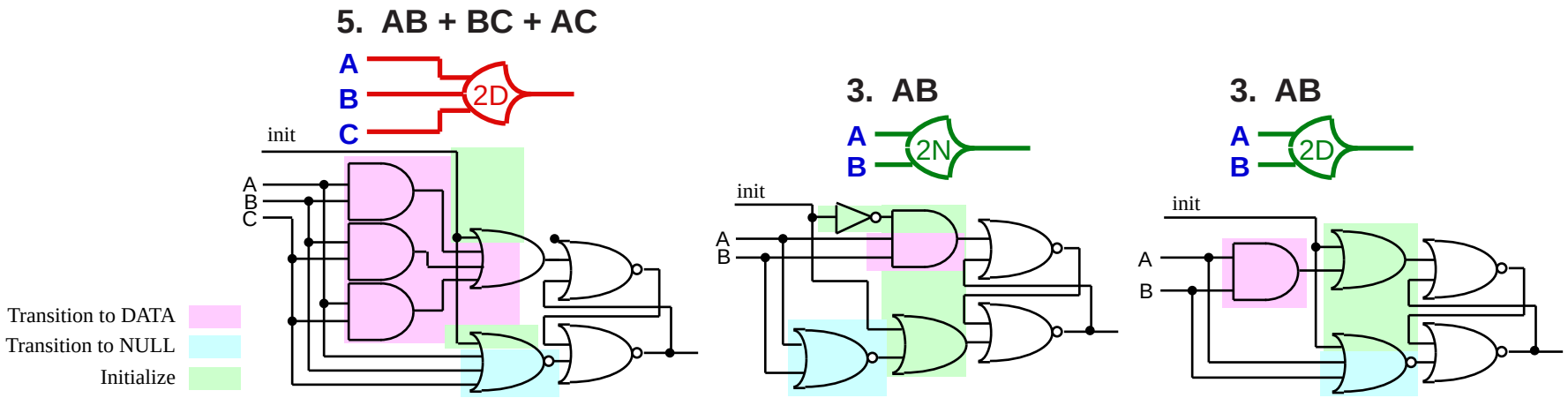
Method One

Initialization to DATA or to NULL



a. General Init to NULL

b. General Init to DATA



a. Init to DATA

b. Init to NULL

c. Init to DATA

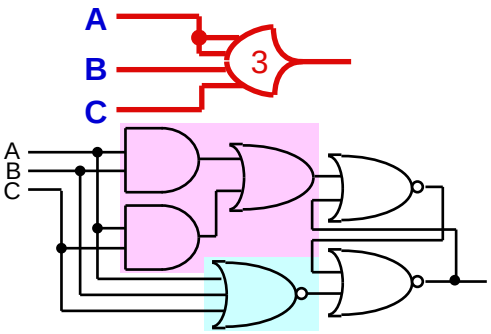
Method One

More examples

Transition to DATA

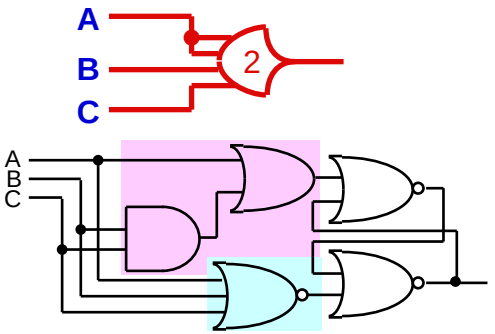
Transition to NULL

8. AB + AC



a. 3of3 W2 operator

7. A + BC



b. 3of3 W2 operator

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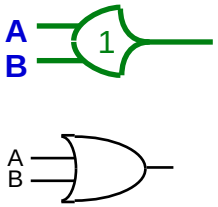
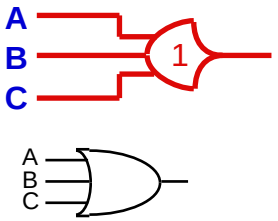
2. A + B



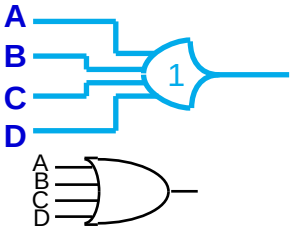
a. 1of2 operator

4. A + B + C



b. 1of3 operator

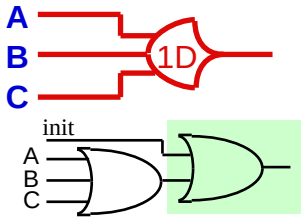
9. A + B + C + D



c. 1of4 operator

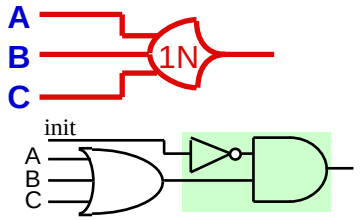
Initialize

4. A + B + C



a. Init to DATA

4. A + B + C



b. Init to NULL

Method Two

Define the NCL gates with logical control

2 of 3 gate

```
module TH23(Z, A, B, C);
output Z;   input A;   input B;   input C;
    logic zi;
      always @(A or B or C)
        begin
          if ((A & B) | (A & C) | (B & C))
            begin #1 zi <= 1; end
          else if ((A==0) & (B==0) & (C==0))
            begin #1 zi <= 0; end
        end
      assign #40 Z = zi;
endmodule
```

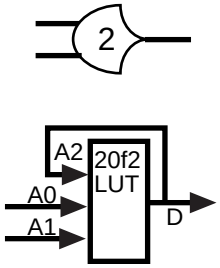
Initialize to DATA

```
module TH22D(Z, A, B, I);
output Z; input A; input B; input I;
  logic zi;
    always @(A or B or I)
      begin
        if (I == 1)
          begin #1 zi <=  1; end
        else
          if (((A) & (B)))
            begin #1 zi <=  1; end
          else if (((A==0) & (B==0)))
            begin #1 zi <=  0; end
      end
  assign #40 Z = zi;
endmodule
```

Method Three

FPGA look-up tables can be directly configured to function as Null Convention Logic (NCL) threshold gates.

Look Up Table Configuration and Behavior

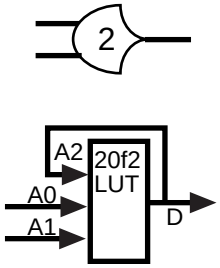


2 of 2

A2	A1	A0	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

the output and A2 remain 0 until both inputs are 1

the output and A2 remain 1 until both inputs are 0



1 of 2

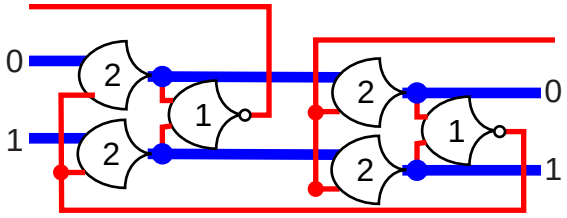
A2	A1	A0	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

the output and A2 remain 0 until one input becomes 1

the output and A2 remain 1 until both inputs are 0

The LUT Feedback Time Relation

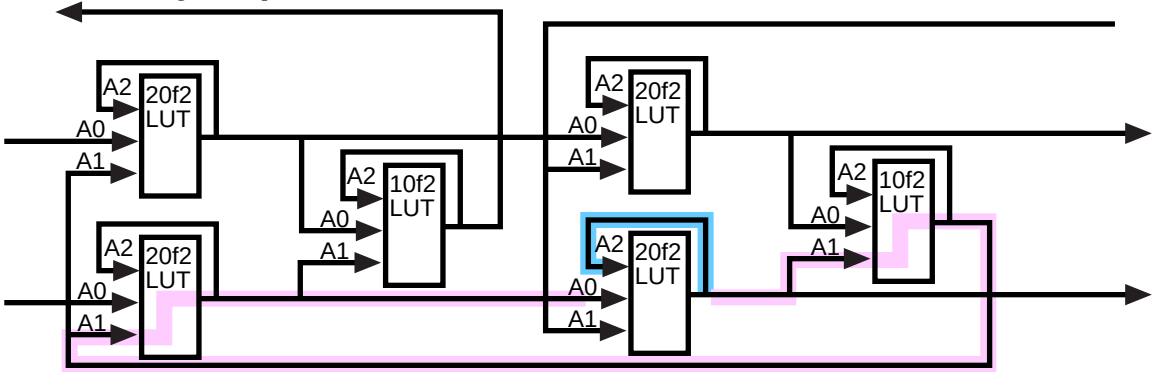
As with any NCL gate the feedback in the gate has to be faster than the path around the cycle



2 of 2

A2	A1	A0	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The cycle path back to A0

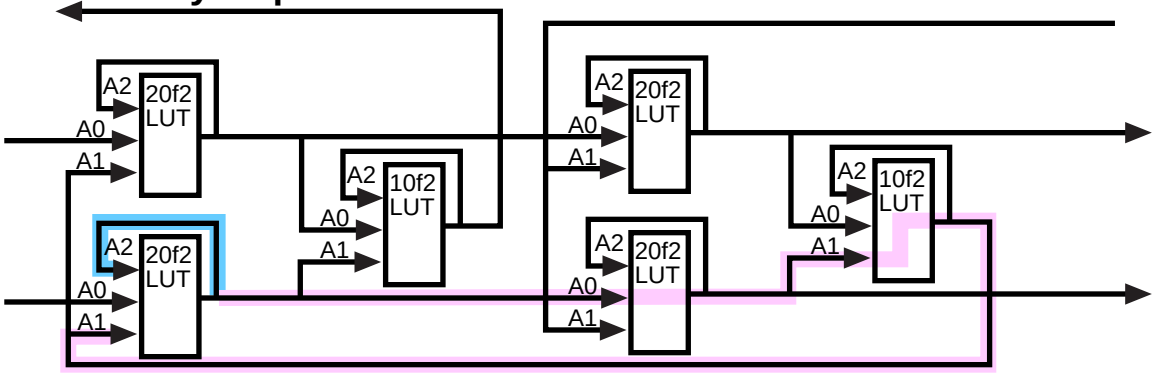


From the branch the blue path has to be faster than the pink path

1 of 2

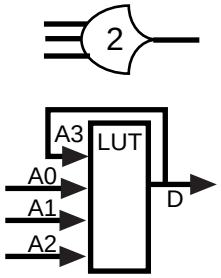
A2	A1	A0	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The cycle path back to A1



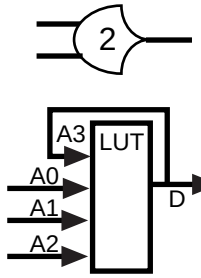
From the branch the blue path has to be faster than the pink path

2 of 3



A3	A2	A1	A0	D
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

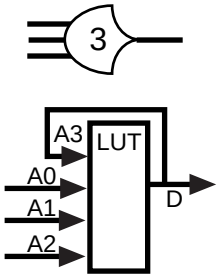
2 of 2 in 4 input LUT



A3	A2	A1	A0	D
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

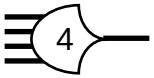
A2 is tied to 0 so the effective mapping is in the A2 = 0 sectors. The A2 = 1 sectors are never addressed.

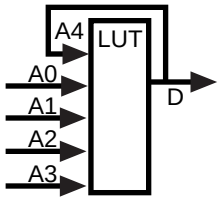
3 of 3



A3	A2	A1	A0	D
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

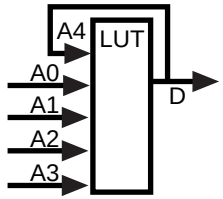
4 of 4





A4	A3	A2	A1	A0	D
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

3 of 5 w2



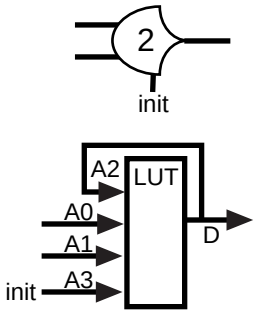
A3 is the weight 2 input.

A4	A3	A2	A1	A0	D
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

Initialized Gates

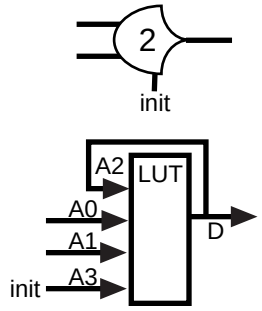
2 of 2 active high init to 1

init	A3	A2	A1	A0	D	
	0	0	0	0	0	
	0	0	0	1	0	
	0	0	1	0	0	
	0	0	1	1	1	
	0	1	0	0	0	
	0	1	0	1	1	
	0	1	1	0	1	
	0	1	1	1	1	normal operation
	1	0	0	0	1	
	1	0	0	1	1	
	1	0	1	0	1	
	1	0	1	1	1	initialize
	1	1	0	0	1	
	1	1	0	1	1	
	1	1	1	0	1	
	1	1	1	1	1	



2 of 2 active low init to 0

init	A3	A2	A1	A0	D	
	0	0	0	0	0	
	0	0	0	1	0	
	0	0	1	0	0	
	0	0	1	1	0	
	0	1	0	0	0	
	0	1	0	1	0	
	0	1	1	0	0	
	0	1	1	1	0	initialize
	1	0	0	0	0	
	1	0	0	1	0	
	1	0	1	0	0	
	1	0	1	1	1	
	1	1	0	0	0	
	1	1	0	1	1	
	1	1	1	0	1	
	1	1	1	1	1	normal operation



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