Logically Determined Design
and
Flow Computing
with
With NULL Convention Logic

First Principles

Karl Fant

Feb, 2015

Materials of this conversation, slides and circuit movie, can be downloaded from karlfant.net/ytvideo

The NULL Convention

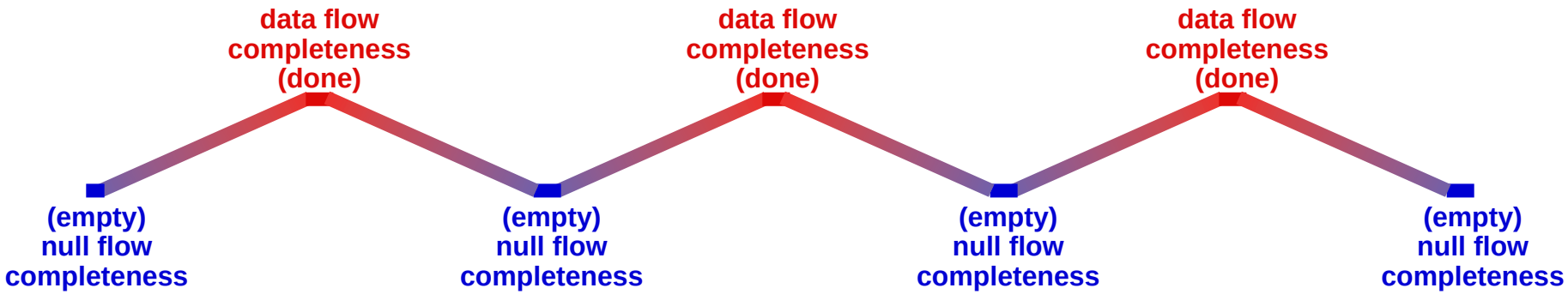
Given an element with two distinct states such as high and low voltage on an electronic wire we assign one state to mean “data” and the other state to mean “not data”, which we will call NULL. This is in contrast to assigning both states a data meaning such as 0,1 or True, False.

The Multi-rail Convention

With only one data state data variables will be multi-rail encoded. A binary variable will be dual-rail encoded with two wires, one meaning 0 the other meaning 1, only one of which will be data at a time.

The Completeness Convention

We define patterns of each state that represent completeness. Consider the output of a dual-rail ripple carry adder which begins with all rails null. Inputs transition to data and output rails begin transitioning to data. When the add is done exactly one rail of each output dual-rail variable has transitioned to data which is a data state completeness pattern upon the occurrence of which the input can begin transitioning to null. All output rails transitoned to null is a null state completeness pattern upon the occurrence of which the input can begin transitioning to data and so on...



NULL Convention Logic (NCL)

A Dual threshold logic with state holding behavior.

Logic operators with a completeness threshold for DATA
and a completeness threshold for NULL:

- transitions its output to DATA only when its data threshold is met,
- transitions its output to NULL only when its input is completely NULL and
- maintains its output when its input is between the two thresholds

2 0f 2

	D	N
D	D	–
N	–	N

3 0f 3

	DD	DN	ND	NN
D	D	–	–	–
N	–	–	–	N

2 0f 3

	DD	DN	ND	NN
D	D	D	D	–
N	–	–	–	N

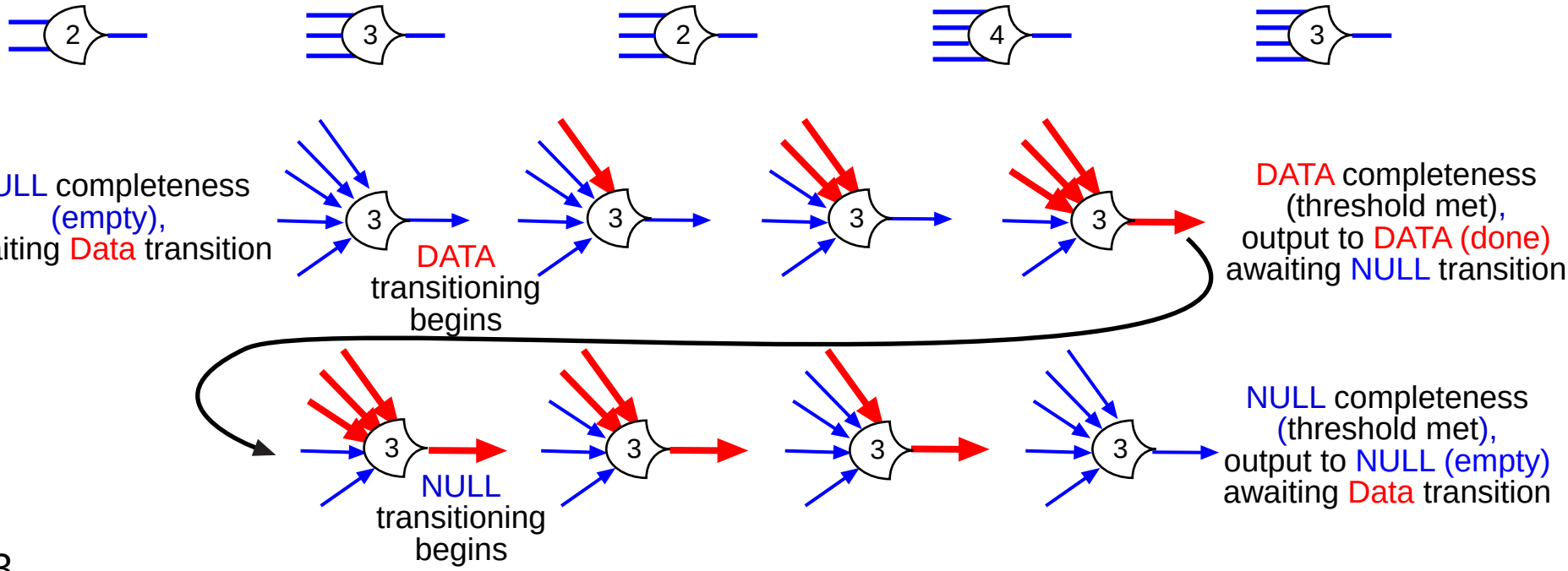
– no transition

4 0f 4

	DD	DN	ND	NN
DD	D	–	–	–
DN	–	–	–	–
ND	–	–	–	–
NN	–	–	–	N

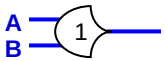
3 0f 4

	DD	DN	ND	NN
DD	D	D	D	–
DN	D	–	–	–
ND	D	–	–	–
NN	–	–	–	N

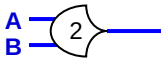


NCL Dual Threshold Logic Functions

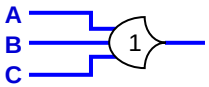
1. A



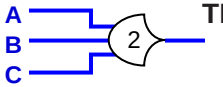
2. A + B



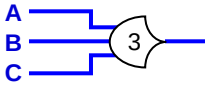
3. AB



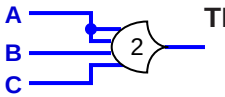
4. A + B + C



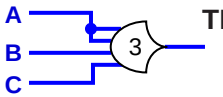
5. AB + BC + AC



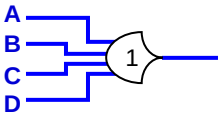
6. ABC



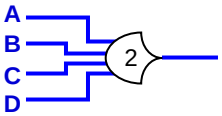
7. A + BC



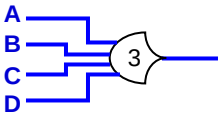
8. AB + AC



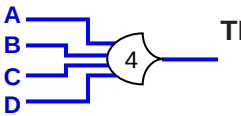
9. A + B + C + D



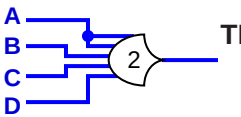
10. AB + AC + AD + BC + BD + CD



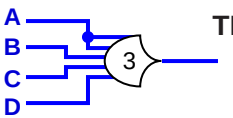
11. ABC + ABD + ACD + BCD



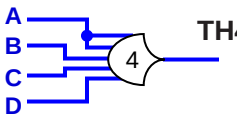
12. ABCD



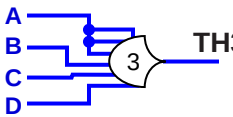
13. A + BC + BD + CD



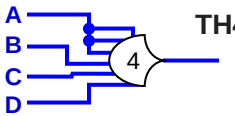
14. AB + AC + AD + BCD



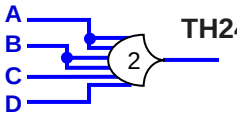
15. ABC + ABD + ACD



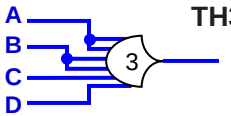
16. A + BCD



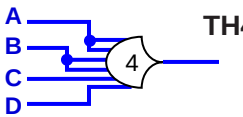
17. AB + AC + AD



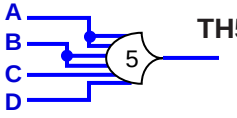
18. A + B + CD



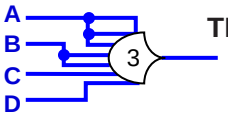
19. AB + AC + AD + BC + BD



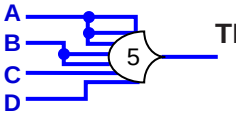
20. AB + ACD + BCD



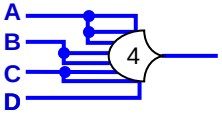
21. ABC + ABD



22. A + BC + BD

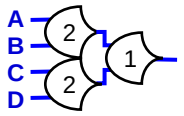


23. AB + ACD

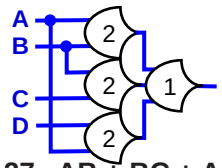


24. AB + AC + AD + BC

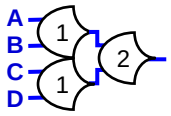
25. AB + AC + BCD



26. AB + CD



27. AB + BC + AD



28. AC + BC + AD + BD

The multi-rail convention

With only one data value, an M value variable is expressed with M rails only one of which will express its DATA value at a time.

Wire	numeric base 2 meanings		
	NULL	0	1
#1	N	D	N
#2	N	N	D

Wire	Logical meanings		
	NULL	TRUE	FALSE
#1	N	D	N
#2	N	N	D

Wire	numeric base 4 meanings				
	NULL	0	1	2	3
#1	N	D	N	N	N
#2	N	N	D	N	N
#3	N	N	N	D	N
#4	N	N	N	N	D

Wire	general meanings			
	NULL	Animal	Vegetable	Mineral
#1	N	D	N	N
#2	N	N	D	N
#3	N	N	N	D

Wire	numeric base 10 meanings										
	NULL	1	2	3	4	5	6	7	8	9	0
#1	N	D	N	N	N	N	N	N	N	N	N
#2	N	N	D	N	N	N	N	N	N	N	N
#3	N	N	N	D	N	N	N	N	N	N	N
#4	N	N	N	N	D	N	N	N	N	N	N
#5	N	N	N	N	N	D	N	N	N	N	N
#6	N	N	N	N	N	N	D	N	N	N	N
#7	N	N	N	N	N	N	N	D	N	N	N
#8	N	N	N	N	N	N	N	N	D	N	N
#9	N	N	N	N	N	N	N	N	N	D	N
#10	N	N	N	N	N	N	N	N	N	N	D

Wire	control meanings			
	NULL	Select A	Select B	Select C
#1	N	D	N	N
#2	N	N	D	N
#3	N	N	N	D

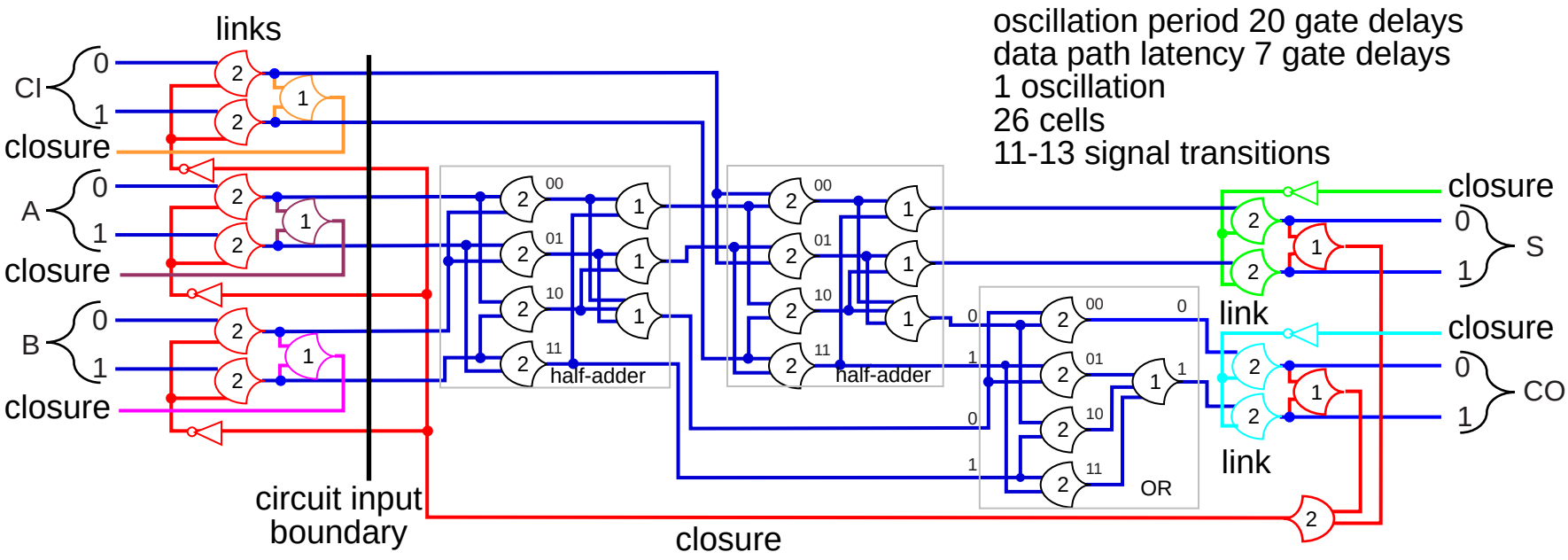
Wire	other meanings				
	NULL	First	Second	Third	Fourth
#1	N	D	N	N	N
#2	N	N	D	N	N
#3	N	N	N	D	N
#4	N	N	N	N	D

Movie discusion

Self Coordination: The Oscillation

Completeness is fed back with inversion (closure) creating an oscillation with:

- one or more sources,
- a completeness flow path and
- one or more destinations



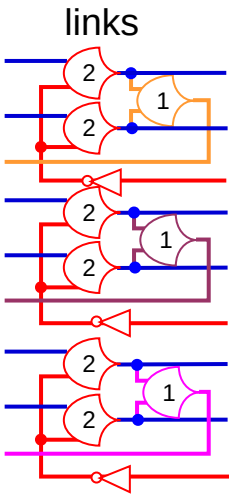
The oscillation Link coordinates flow from oscillation to oscillation

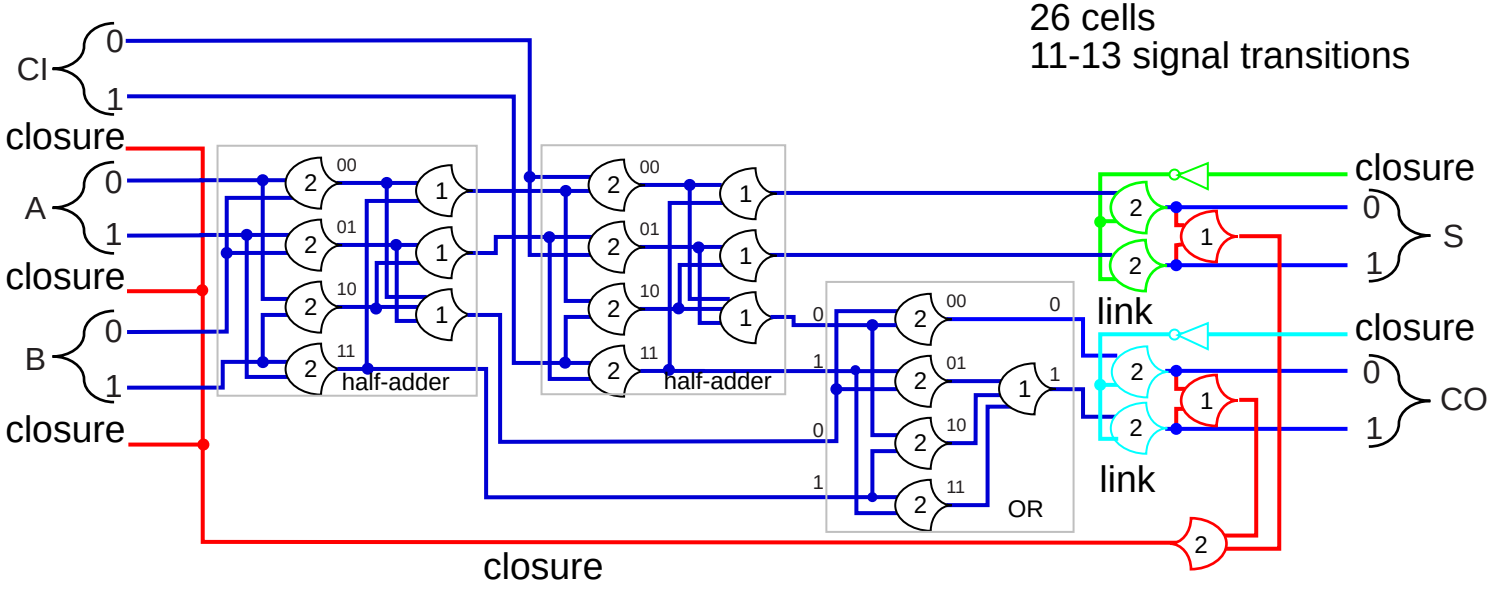
When linked oscillations present data to a link it will pass a data wave and maintain the data wave until the oscillations present null
When linked oscillations present null to a link it will pass a null wave and maintain the null wave until the oscillations present data

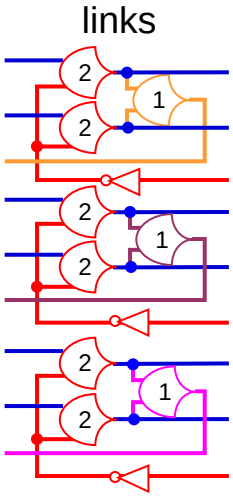
The expression is purely in terms of logical relationships

Since the combinational expression and the link are both in terms of logical relations they can be optimized together

oscillation period 20 gate delays
data path latency 7 gate delays
1 oscillation
26 cells
11-13 signal transitions

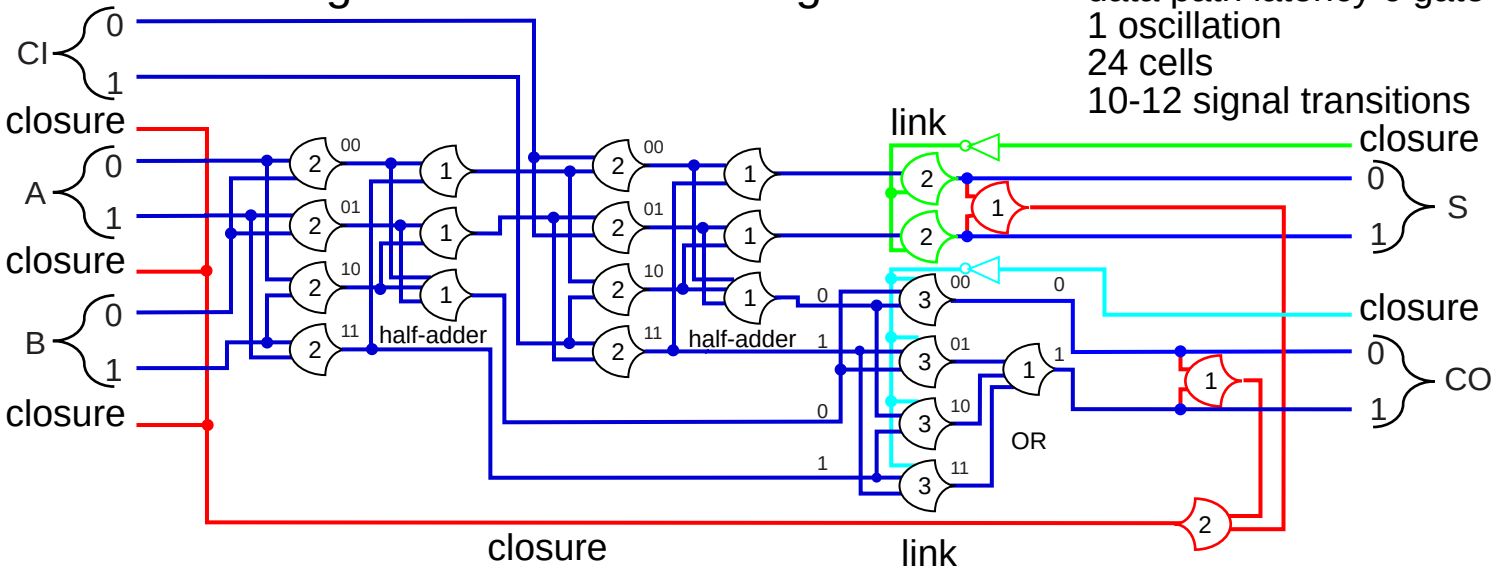




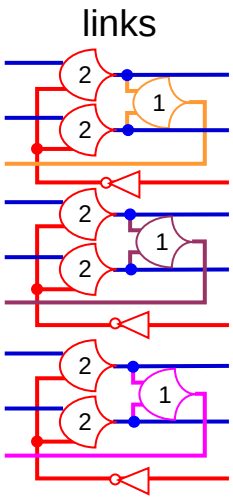


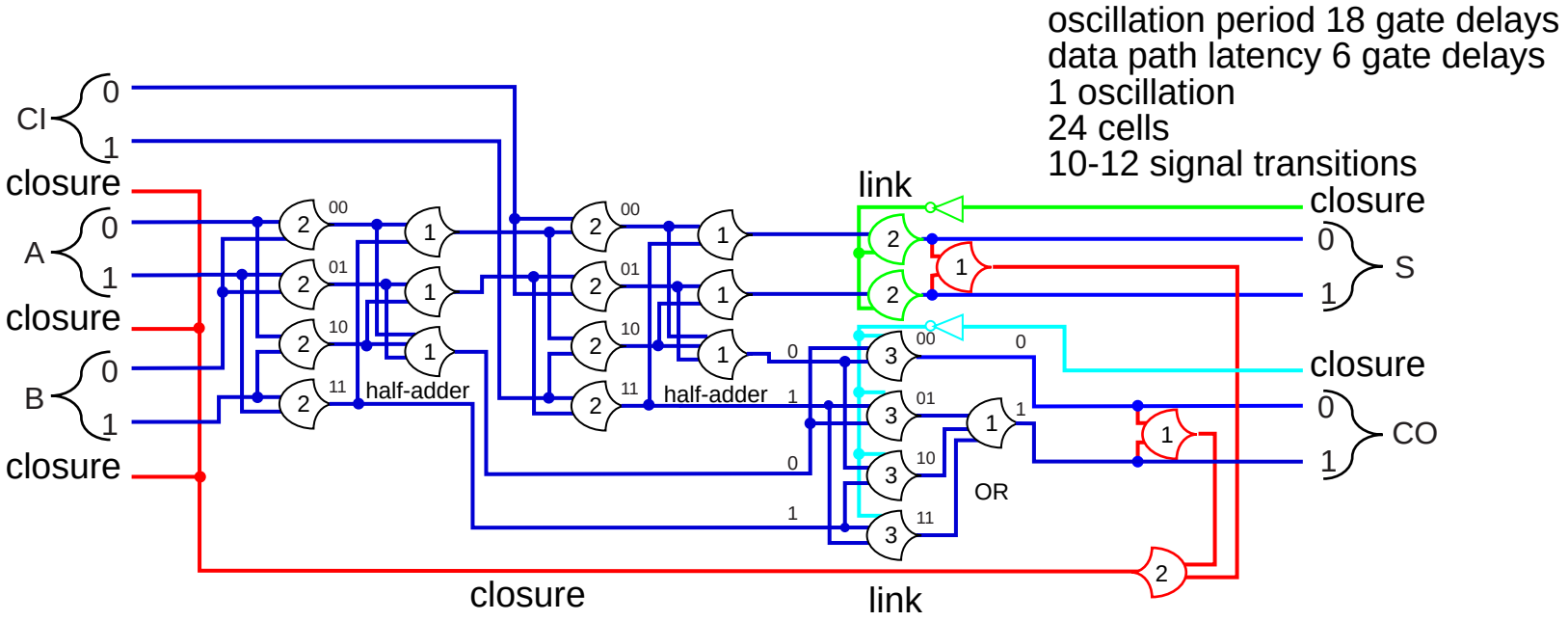
integrate combinational logic and link

oscillation period 18 gate delays
data path latency 6 gate delays
1 oscillation
24 cells
10-12 signal transitions

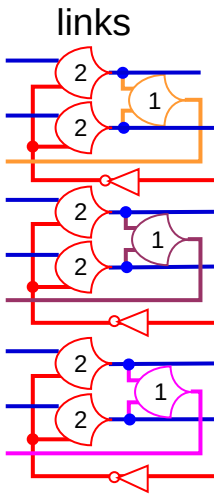


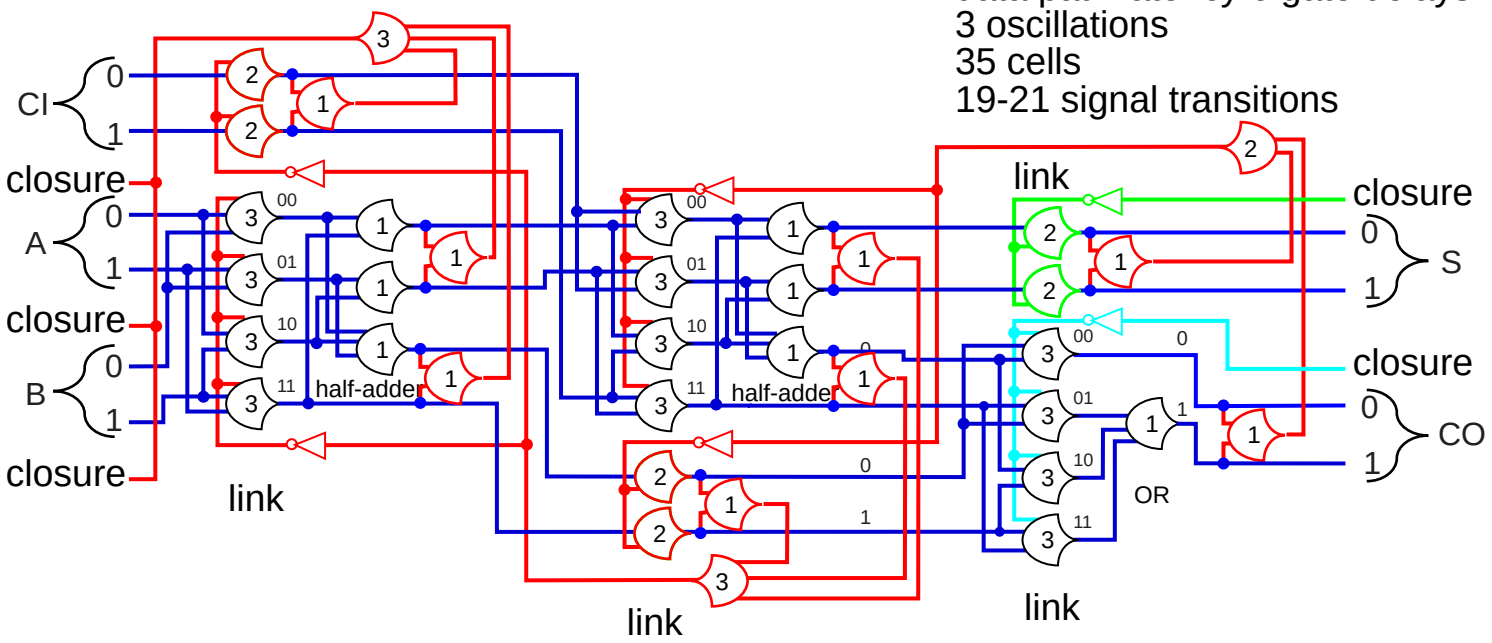
Other combinational ranks can be made a link



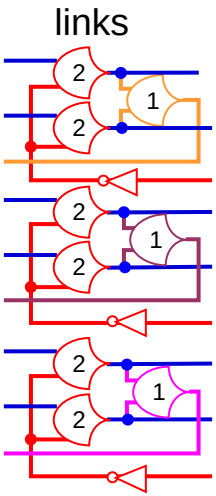


finer oscillation granularity

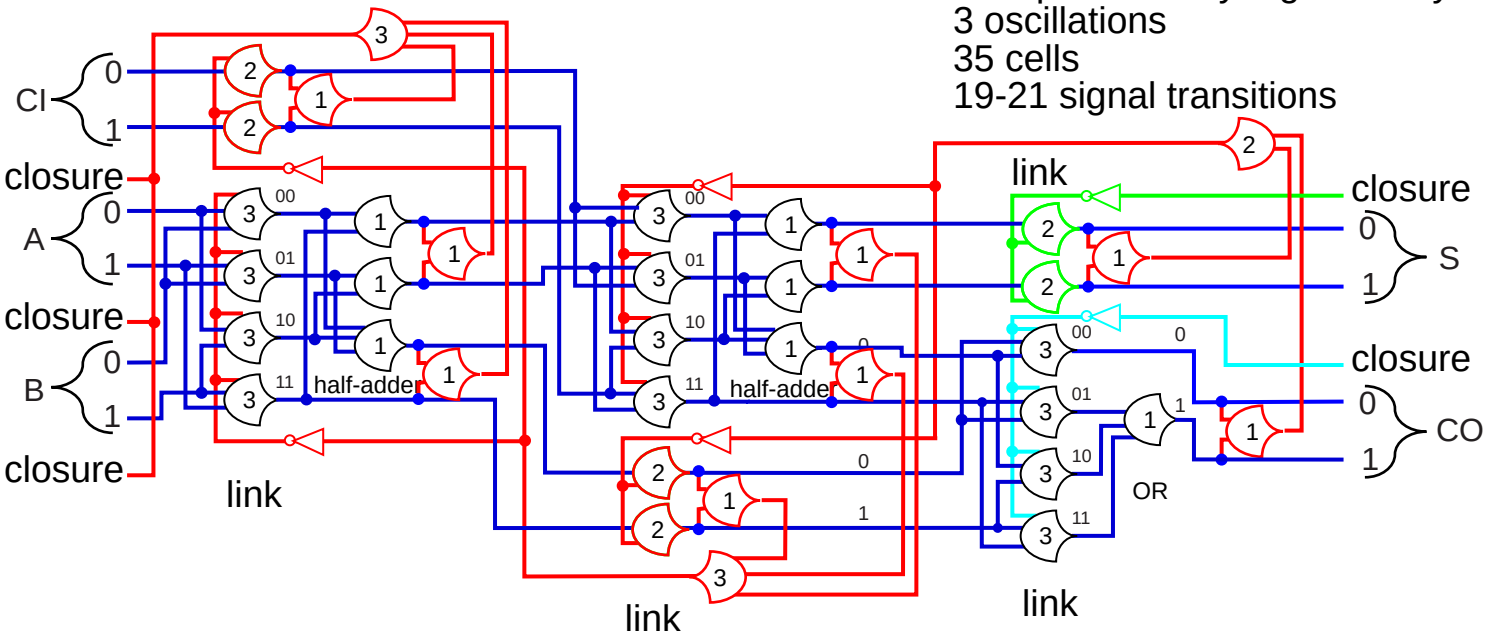




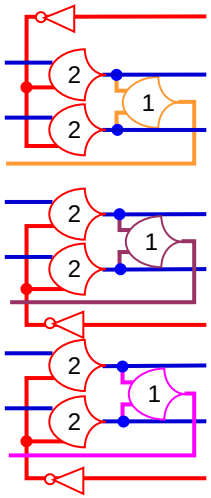
Any combinational rank can be made a link



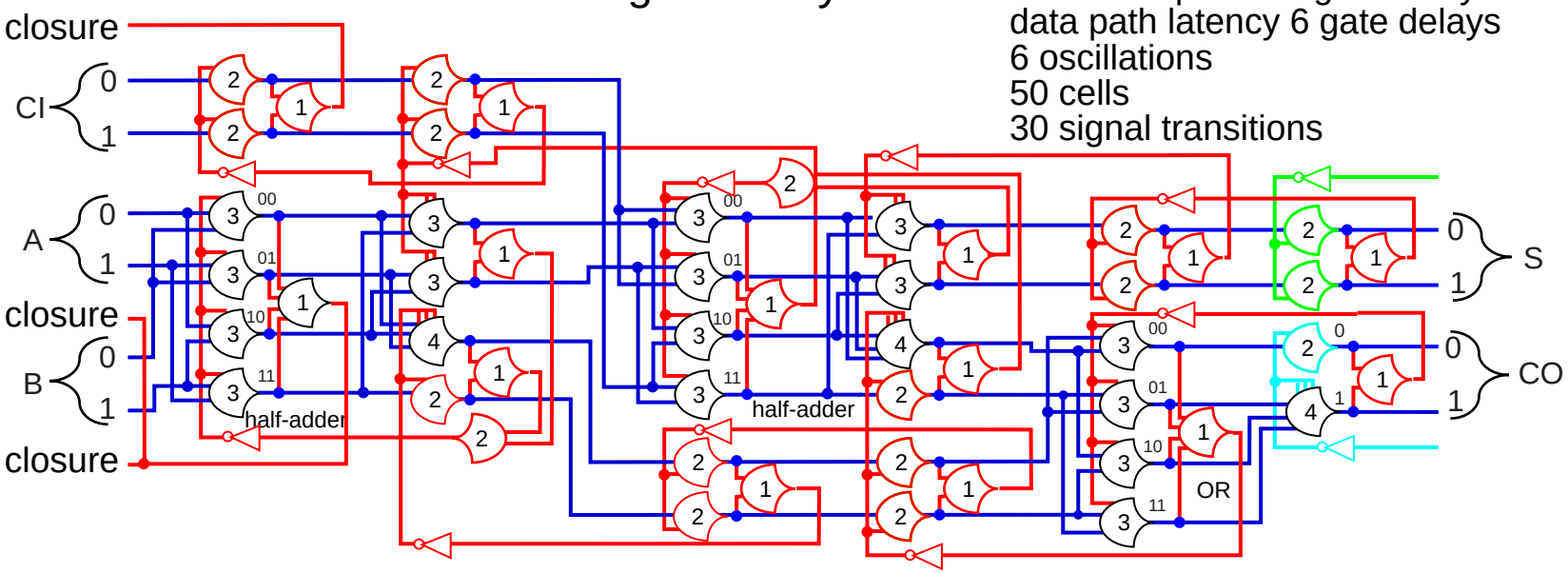
oscillation period 12 gate delays
data path latency 6 gate delays
3 oscillations
35 cells
19-21 signal transitions



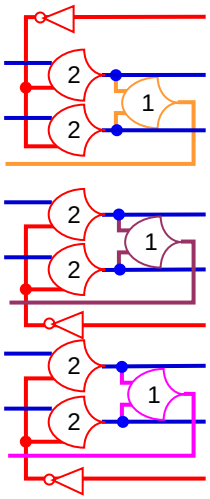
finest oscillation granularity

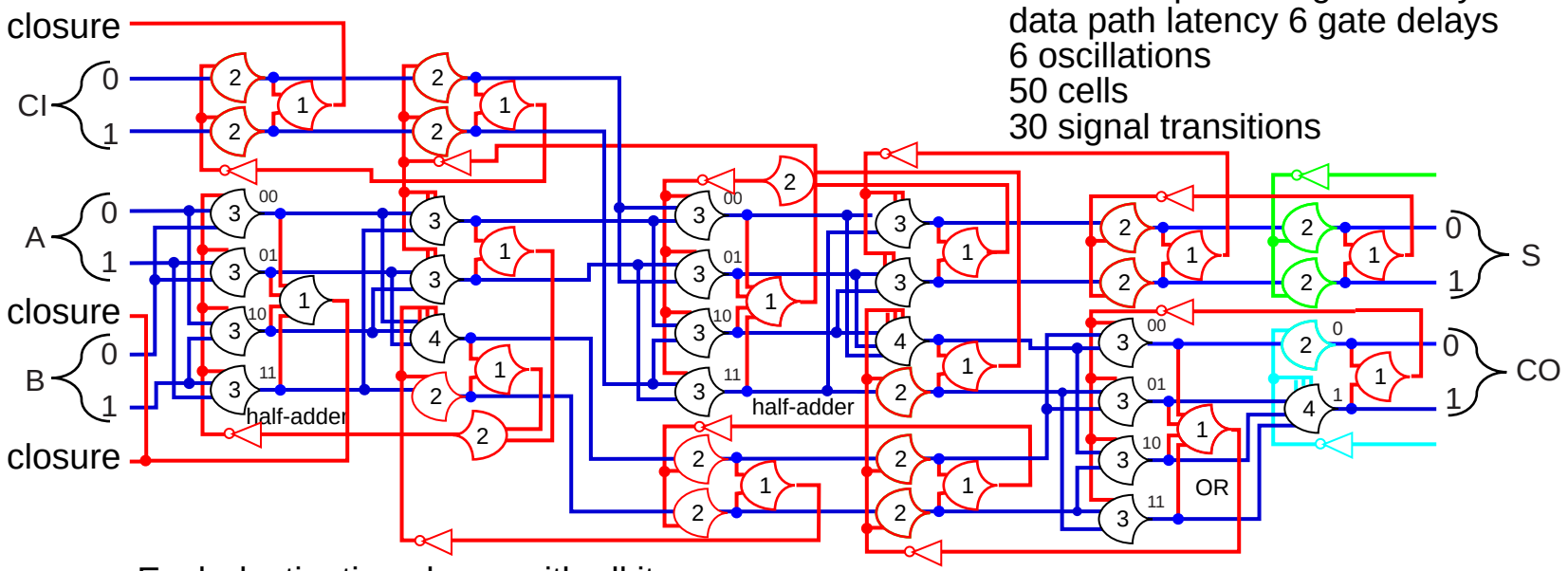


oscillation period 8 gate delays
data path latency 6 gate delays
6 oscillations
50 cells
30 signal transitions

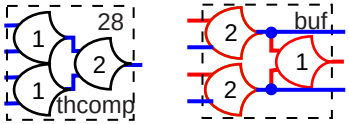


The oscillation structure can be optimized in terms of the logic

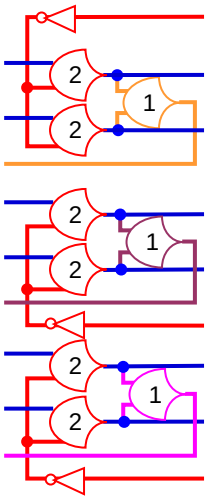


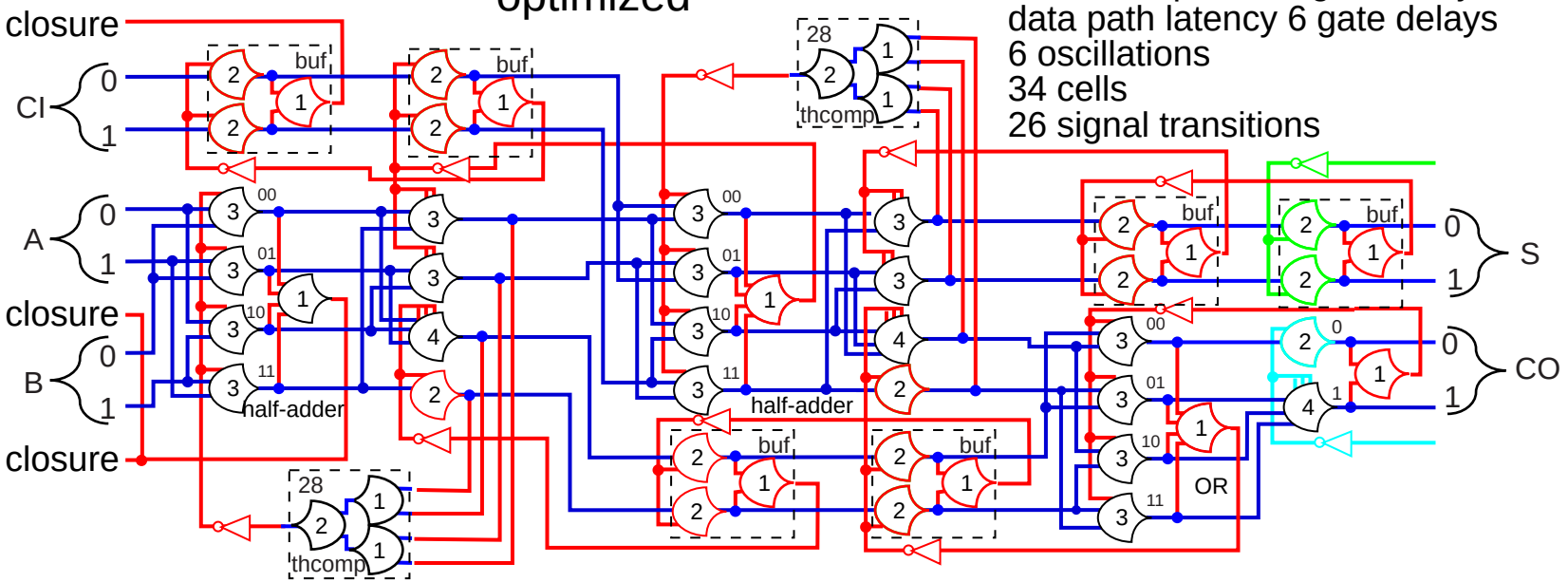


Each destination closes with all its sources
Each source is closed by all its destinations
Each link is both destination and source

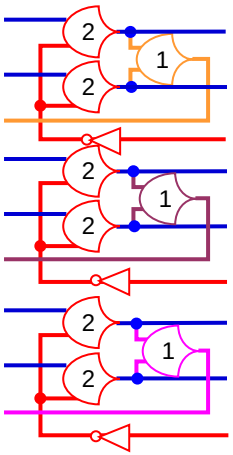


finest oscillation granularity optimized



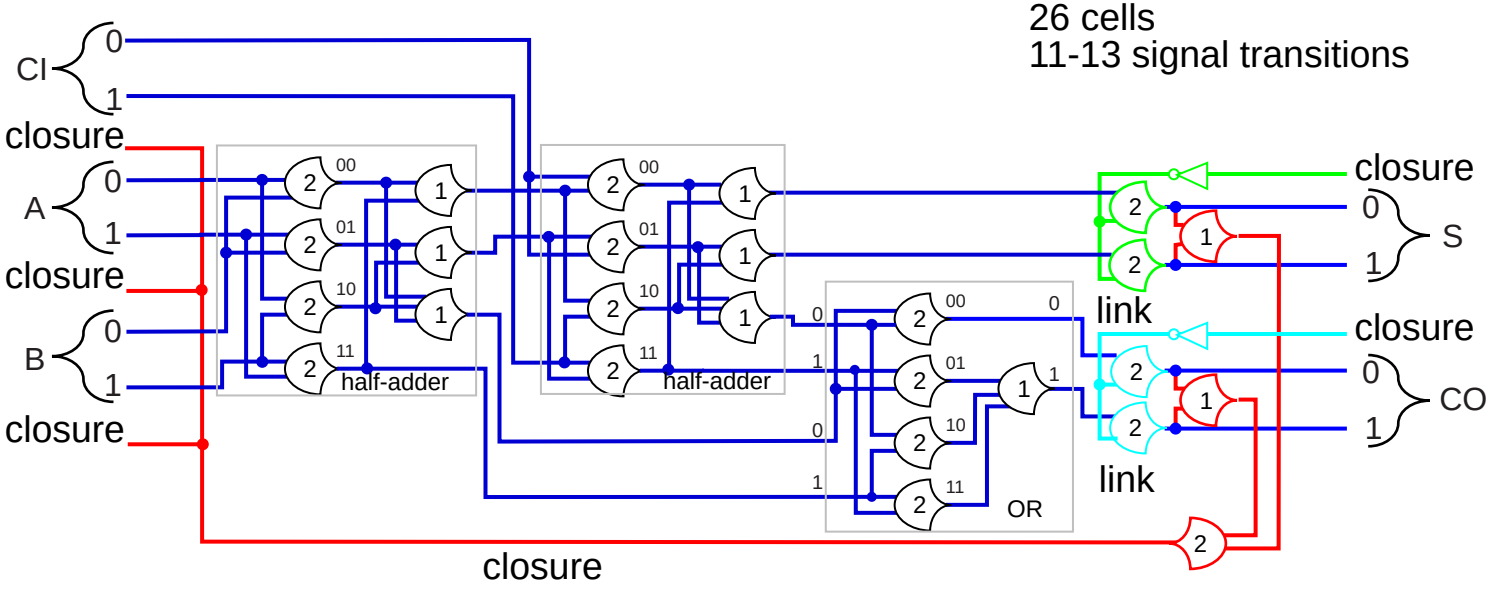


links



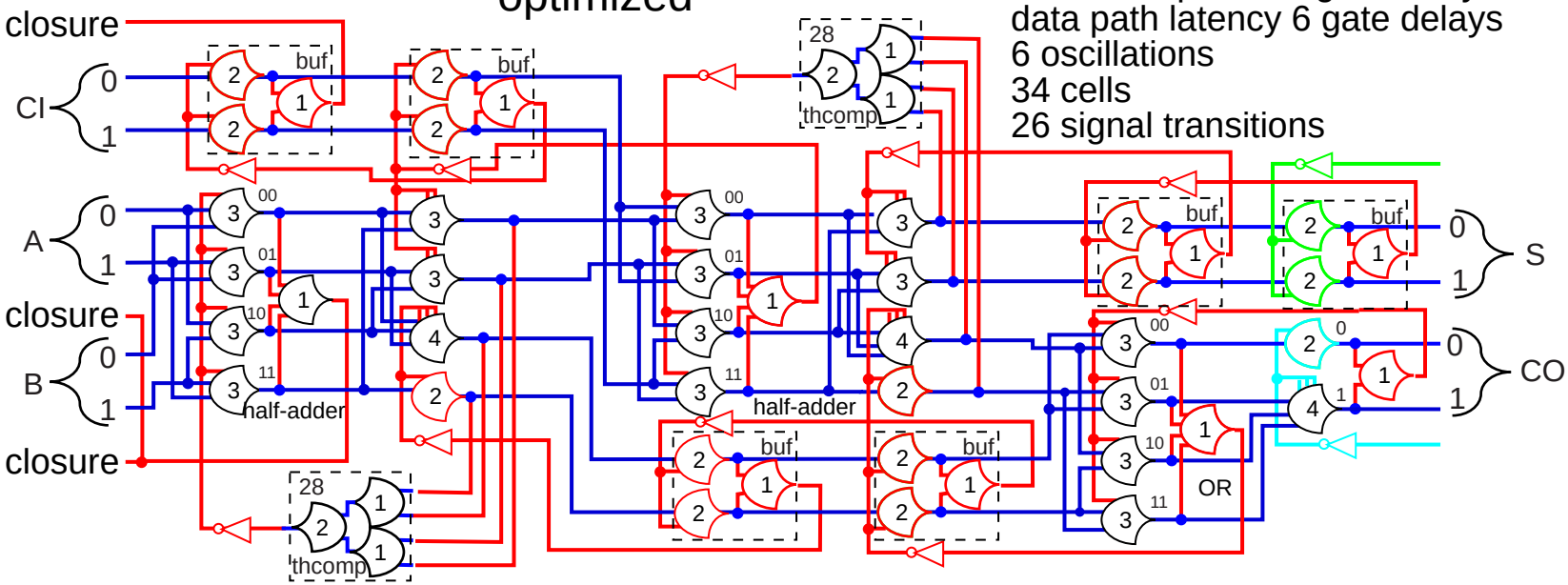
coarsest oscillation granularity
unoptimized

oscillation period 20 gate delays
data path latency 7 gate delays
1 oscillation
26 cells
11-13 signal transitions



finest oscillation granularity
optimized

oscillation period 6 gate delays
data path latency 6 gate delays
6 oscillations
34 cells
26 signal transitions



Logically Determined Design
and
Flow Computing
with
With NULL Convention Logic

First Principles

Karl Fant

Feb, 2015

Materials of this conversation, slides and circuit movie, can be downloaded from karlfant.net/ytvideo