Presentation Slides

Chapter 7

State Machines

Logically Determined Design:
Clockless System Design With NULL Convention Logic

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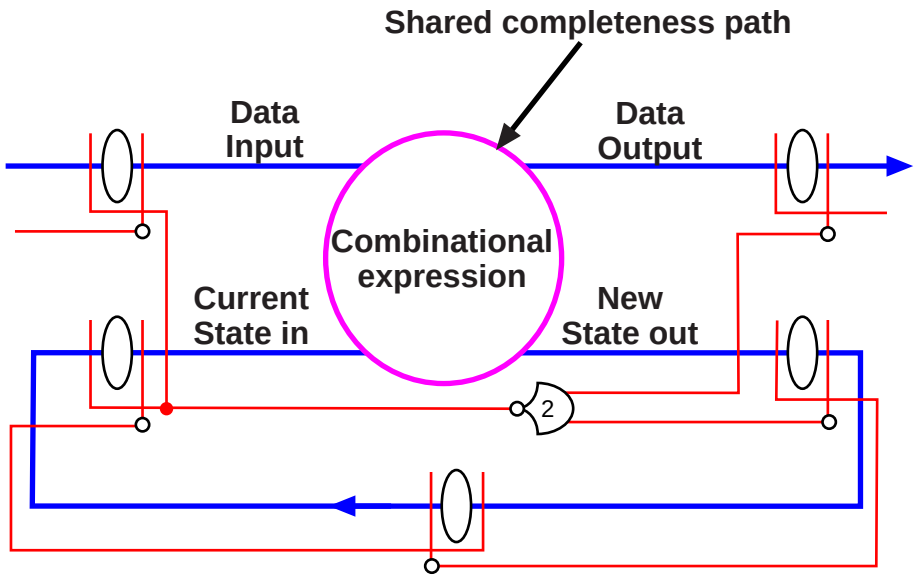
John Wiley & Sons, Inc.

Basic NCL State Machine Structure

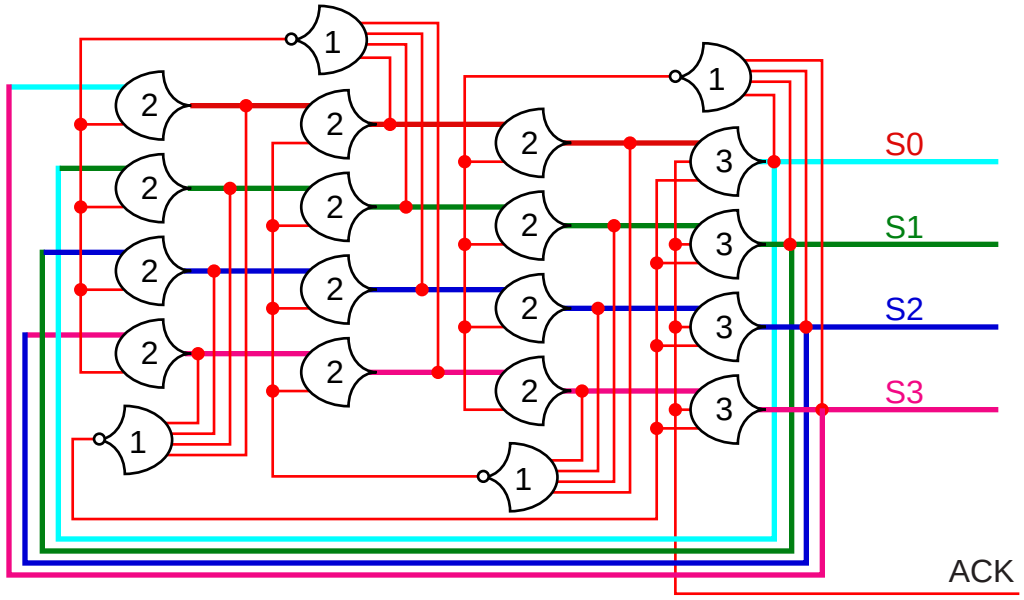
An NCL sequential circuit just like the classic sequential circuit is a combinational circuit with a feedback memory element.

A pipeline (input) coupled to a ring (memory) through a shared completeness path which is the updating combinational expression.



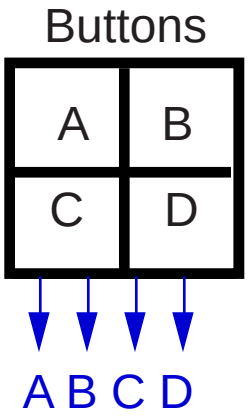
The input data is combined with the current internal state to determine the new state and the functional output. The new state is fedback through the pipeline ring to become the current state for the next input data wavefront.

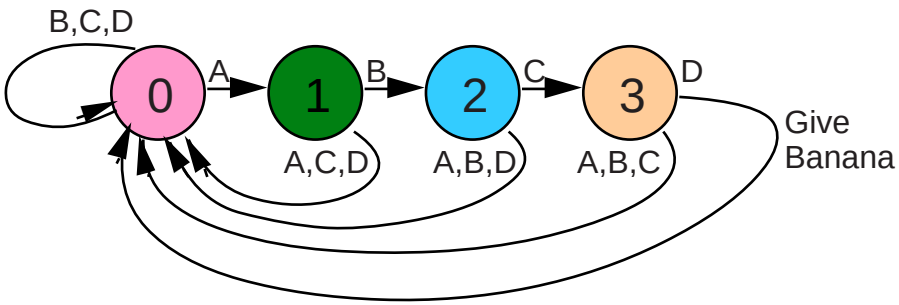
State Sequencer



Monkey Get Banana

- Monkey must press A,B,C,D in that order to get a Banana
- Any out-of-sequence press forces him to start over





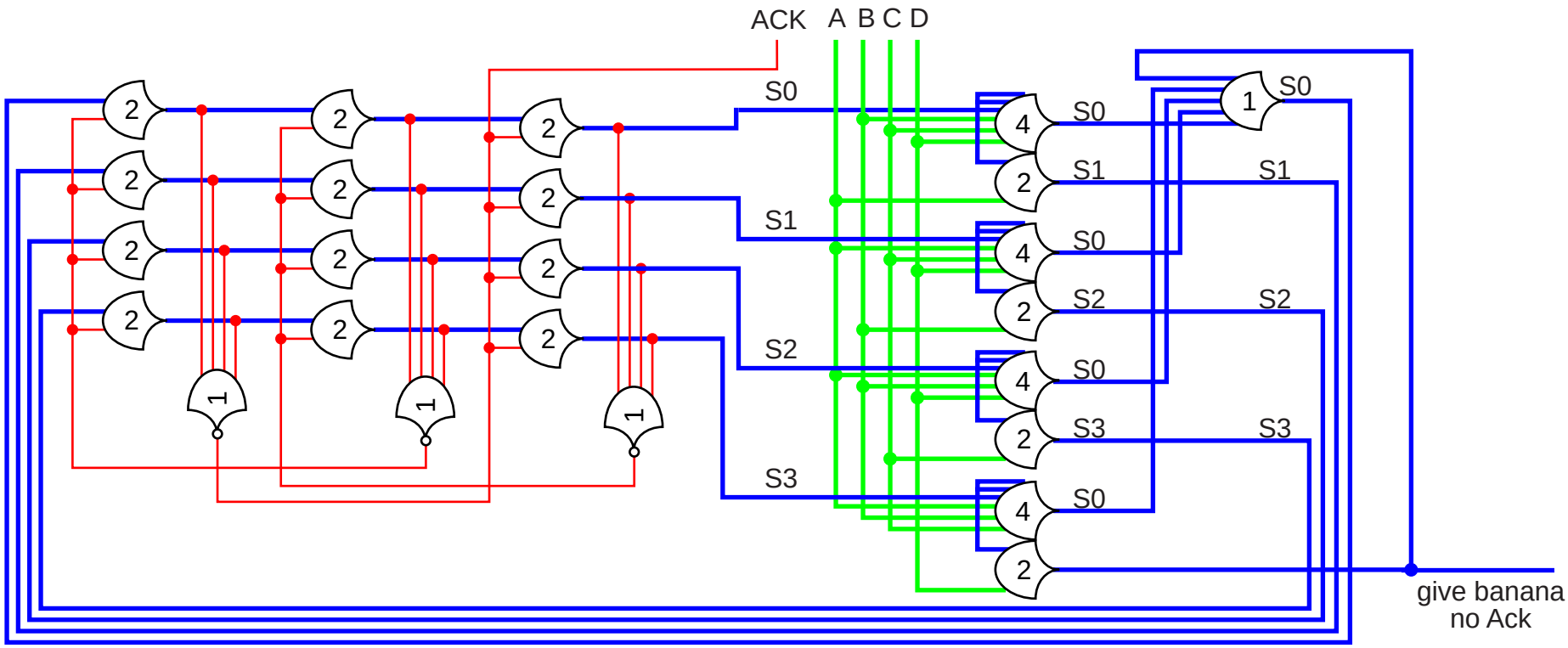
Next state function map

	state 0	state 1	state 2	state 3
A	to state 1	to state 0	to state 0	to state 0
B	to state 0	to state 2	to state 0	to state 0
C	to state 0	to state 0	to state 3	to state 0
D	to state 0	to state 0	to state 0	to state 0 Give Banana

state 0	(0B+0C+0D)+(1A+1C+1D)+(2A+2B+2D)+(3A+3B+3C)+3D
state 1	0A
state 2	1B
state 3	2C
Give Banana	3D

Monkey Get Banana

Complete state machine with the combinational circuit in a three stage ring. It is not feasibile to embed registration because the combinational gates are already four input. We would have to decompose gates to include the Acknowledge signal so embedding registration would not save gates.

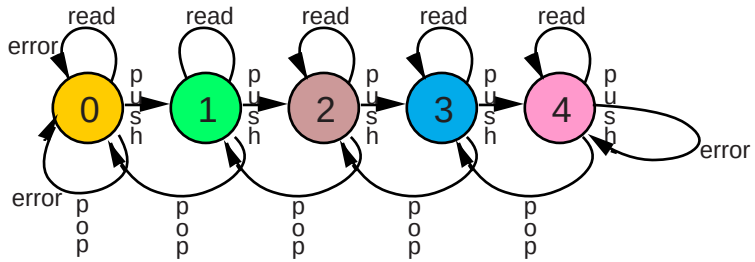


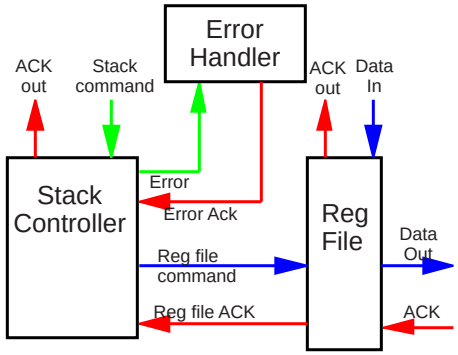
Stack Controller

The state machine maintains the current top of the stack for each command it sends an address and command to the register file and sets the next state. For the empty and full conditions it outputs an error code.

A 4 entry stack with push, pop and read commands
The states are the address lines to the register file.

state machine diagram





next state function map

	state 0	state 1	state 2	state 3	state 4
read	ERROR to state 0	READ to state 1	READ to state 2	READ to state 3	READ to state 4
pop	ERROR to state 0	READ to state 0	READ to state 1	READ to state 2	READ to state 3
push	WRITE to state 1	WRITE to state 2	WRITE to state 3	WRITE to state 4	ERROR to state 4

State 0 is the empty state

State 4 is the full state

state 0 S0read+S0pop+S1pop

state 1 S1read+S0push+S2pop

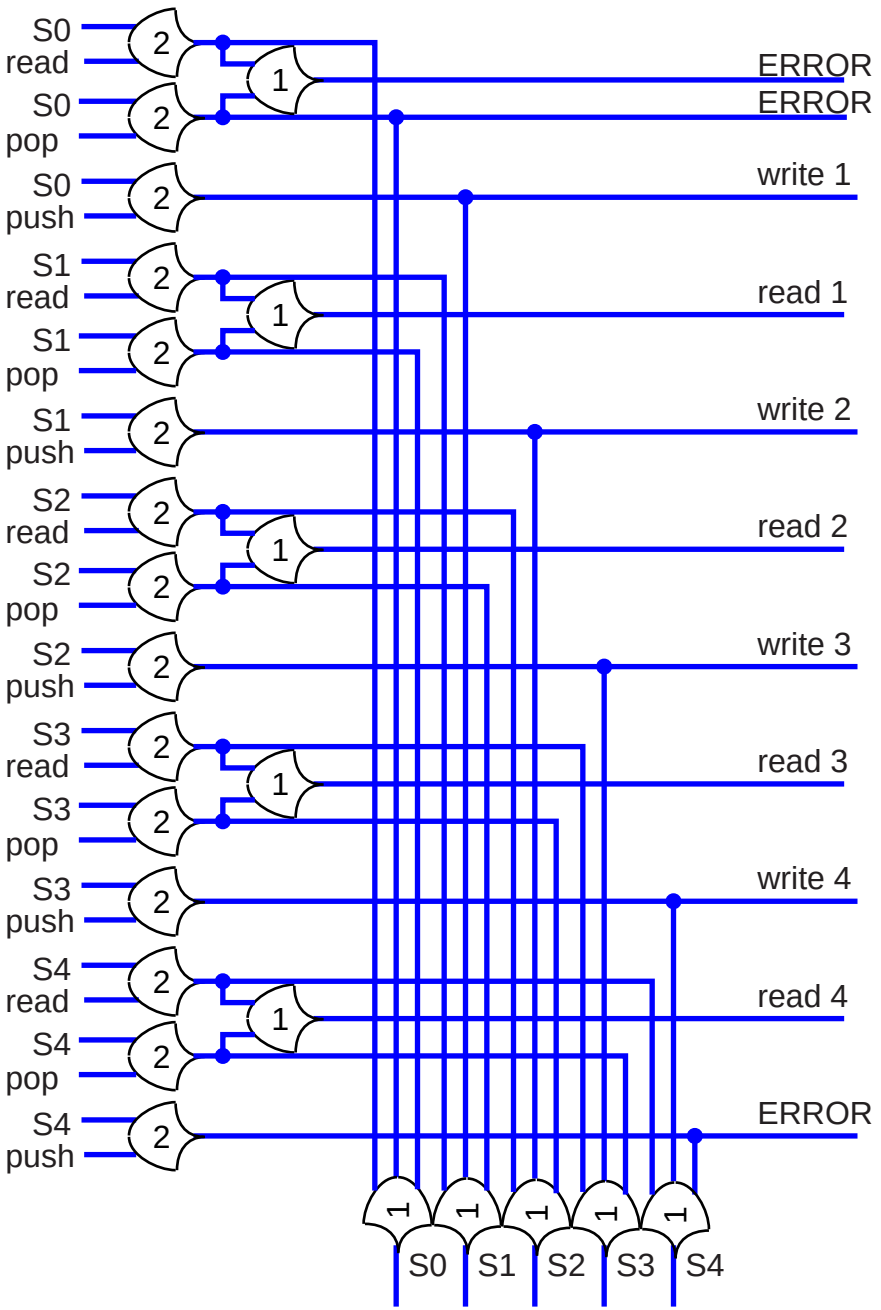
state 2 S2read+S1push+S3pop

state 3 S3read+S2push+S4pop

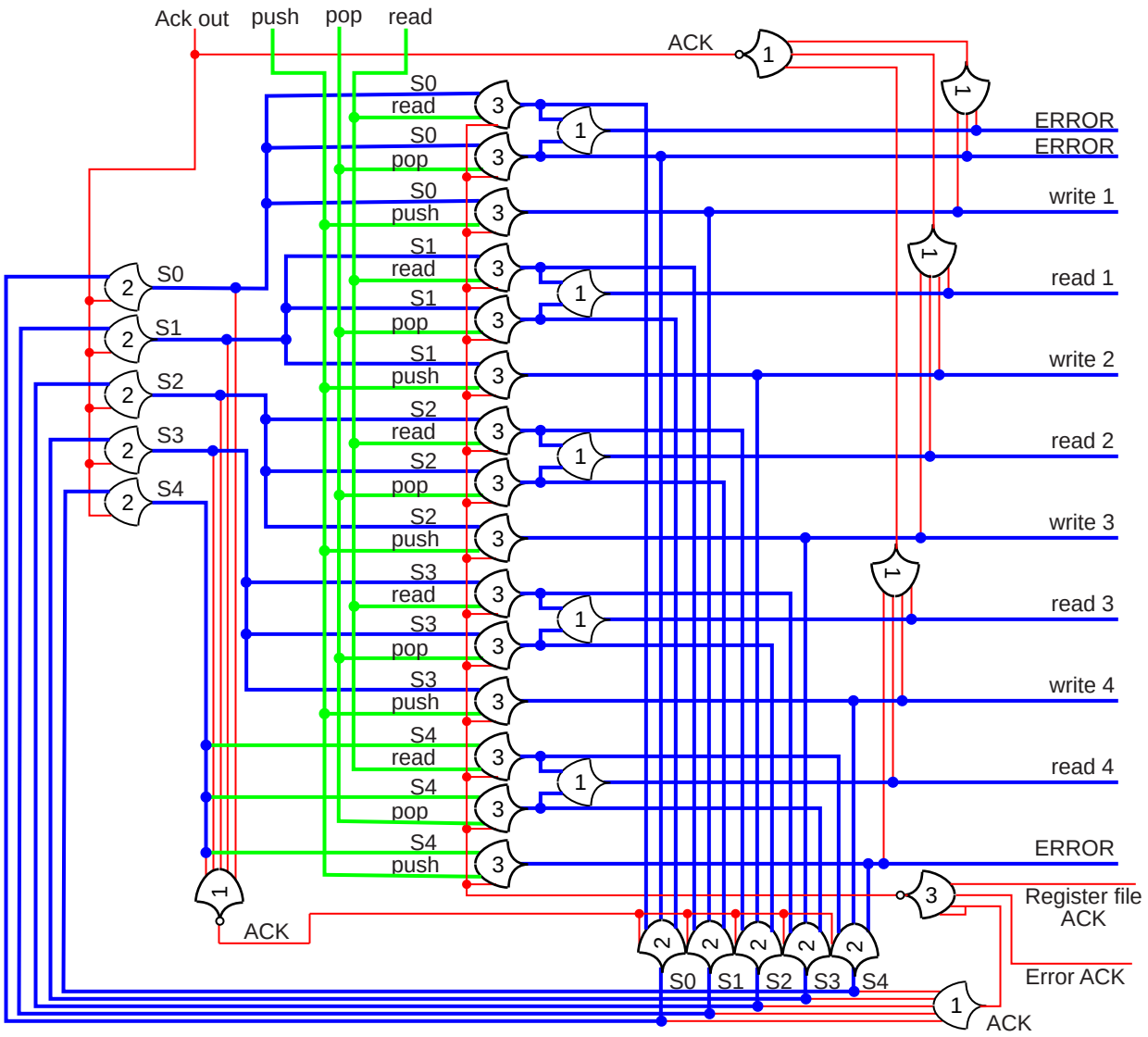
state 4 S4read+S3push+S4push

Stack Controller Combinational Circuit

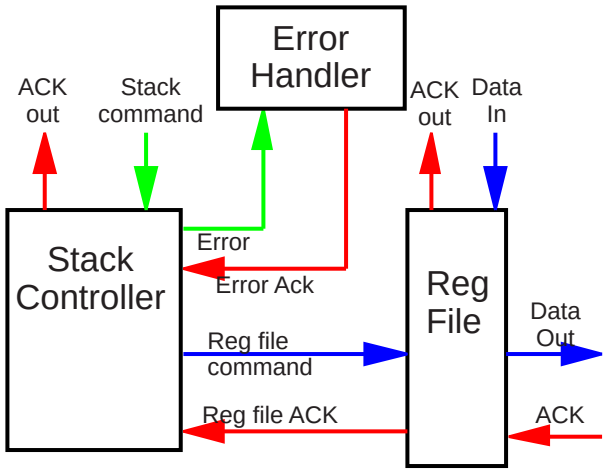
Both ranks of Logic can become embedded completeness/acknowledge stages in the feedback ring.



Stack Controller State Machine



stack controller state machine



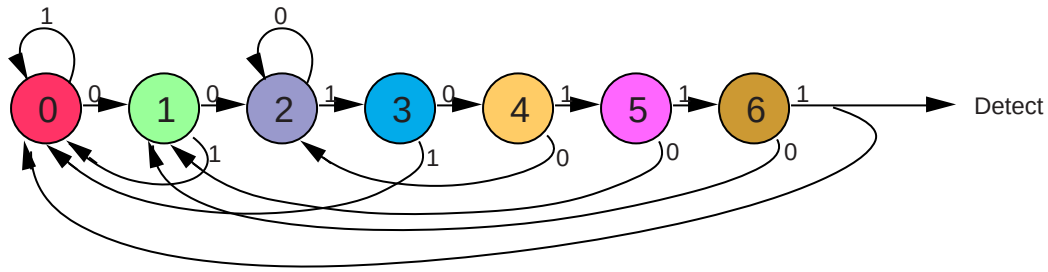
stack controller interface

Code Detector State Machine

review

Detect the sequence 0010111 in a continuous bit stream

seven states S1 thru S6 all states output No-Detect except S6 which outputs Detect

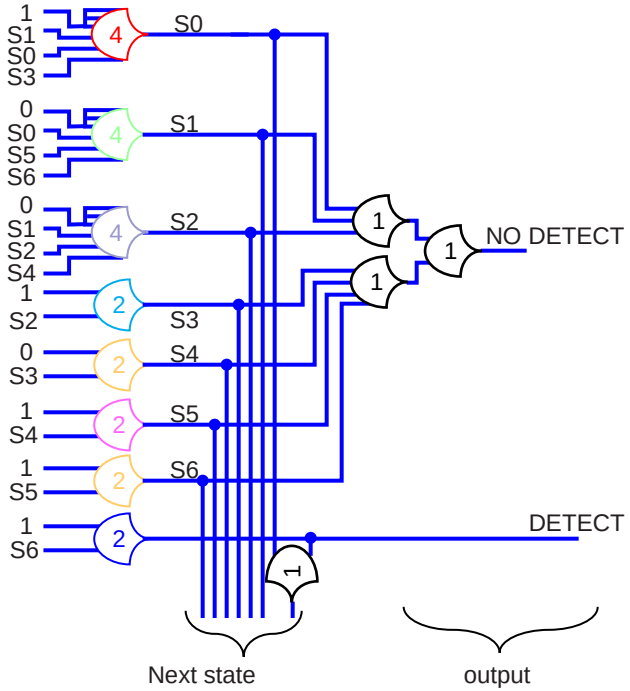


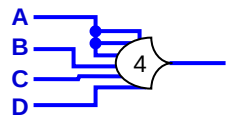
a. state machine diagram

	state 0	state 1	state 2	state 3	state 4	state 5	state 6
0	to state 1	to state 2	to state 2	to state 4	to state 2	to state 1	to state 1
1	to state 0	to state 0	to state 3	to state 0	to state 5	to state 6	to state 0 Detect

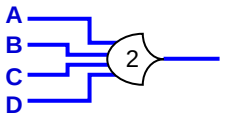
b. Next state function map

	Specific equations	Generic equations
state 0	1S0 + 1S1 + 1S3 + 1S6	AB + AC + AD + AB
state 1	0S0 + 0S5 + 0S6	AB + AC + AD
state 2	0S1 + 0S2 + 0S4	AB + AC + AD
state 3	1S2	AB
state 4	0S3	AB
state 5	1S4	AB
state 6	1S5	AB
detect	1S6	
no detect	everything else	



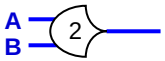


17. AB + AC + AD



10. AB + AC + AD + ~~BC~~ + ~~BD~~ + ~~CD~~

B, C and D are ME

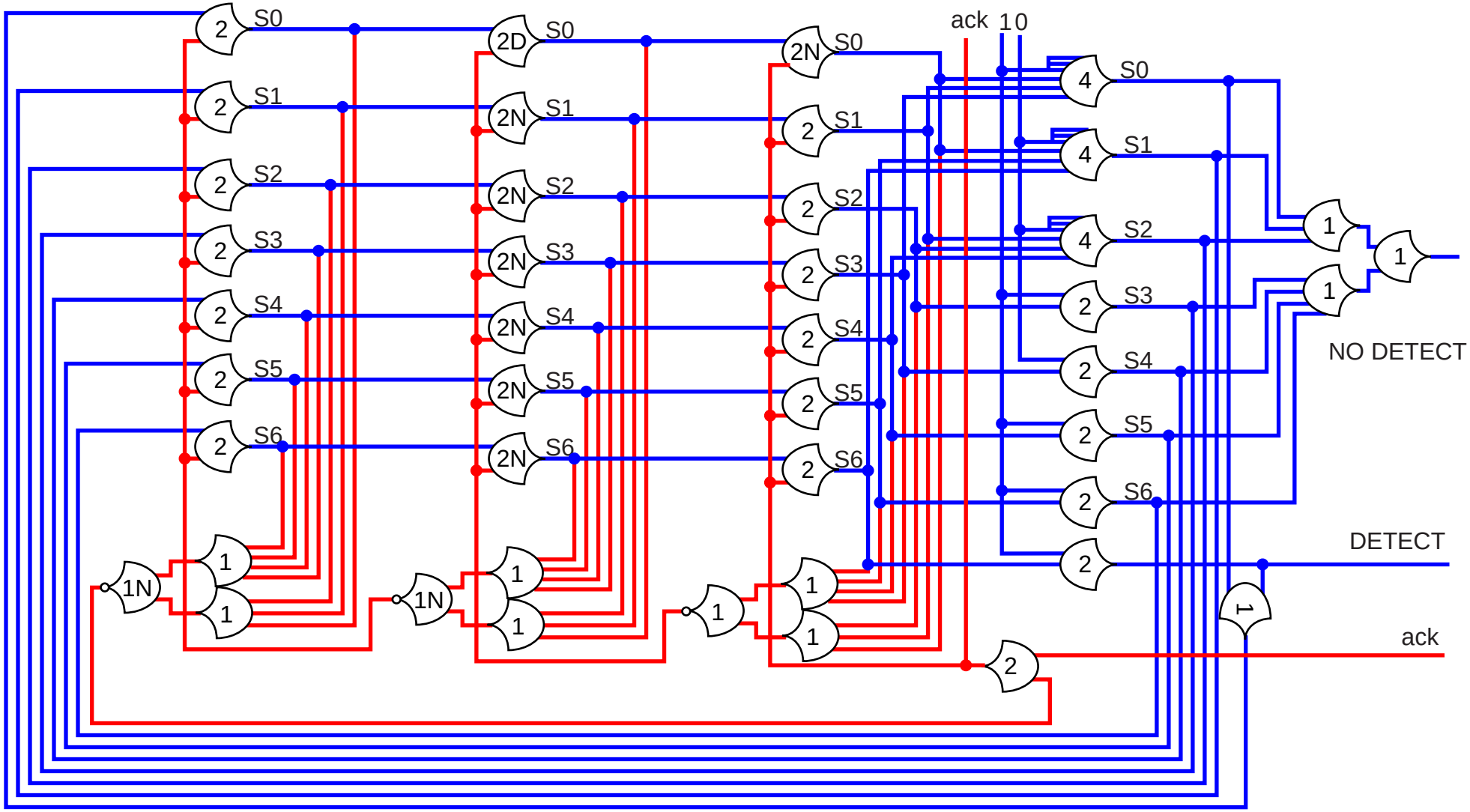


3. AB

7 value variable and 2 value variable to 7 value variable and 2 value variable

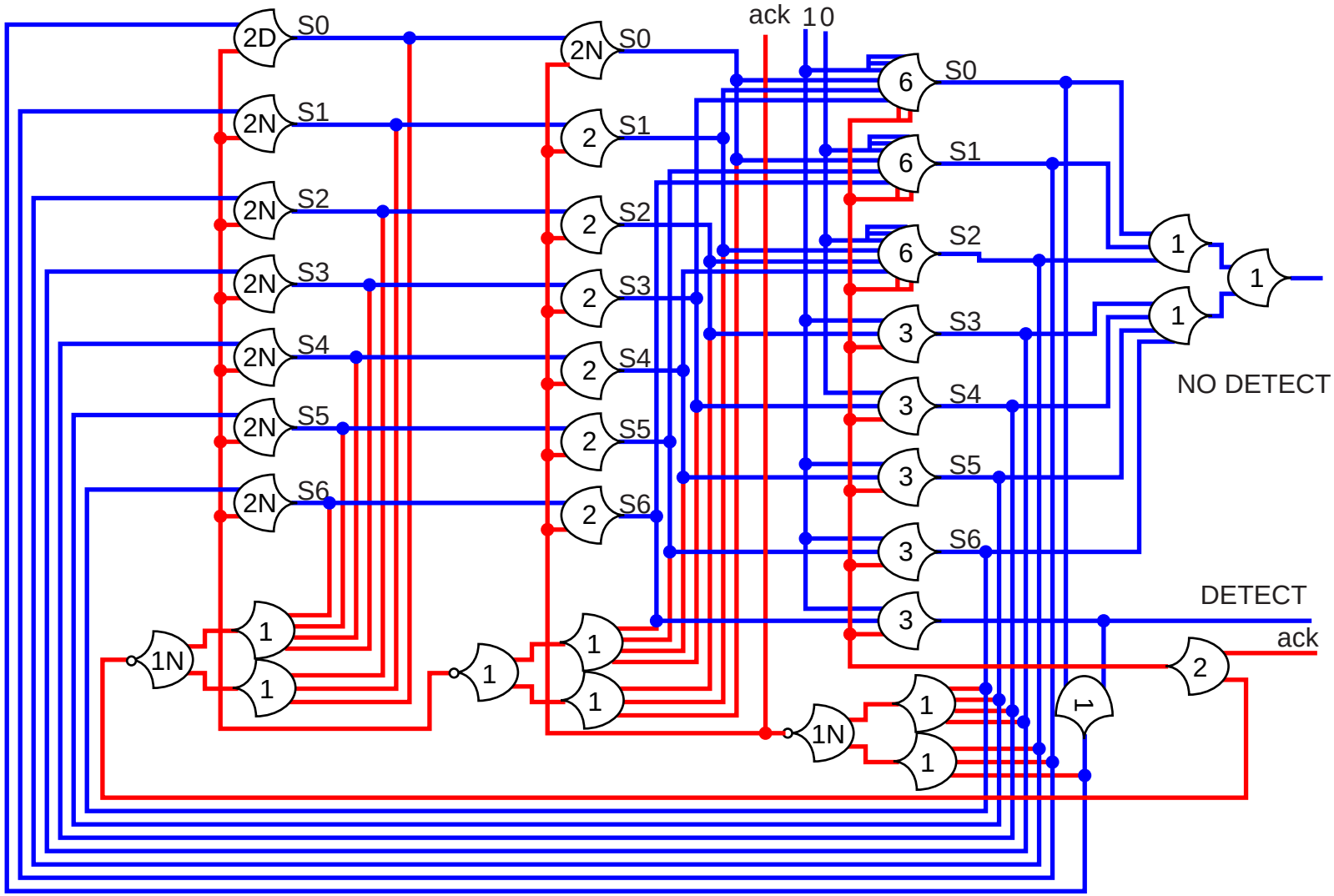
Code Detector State Machine

Initial configuration



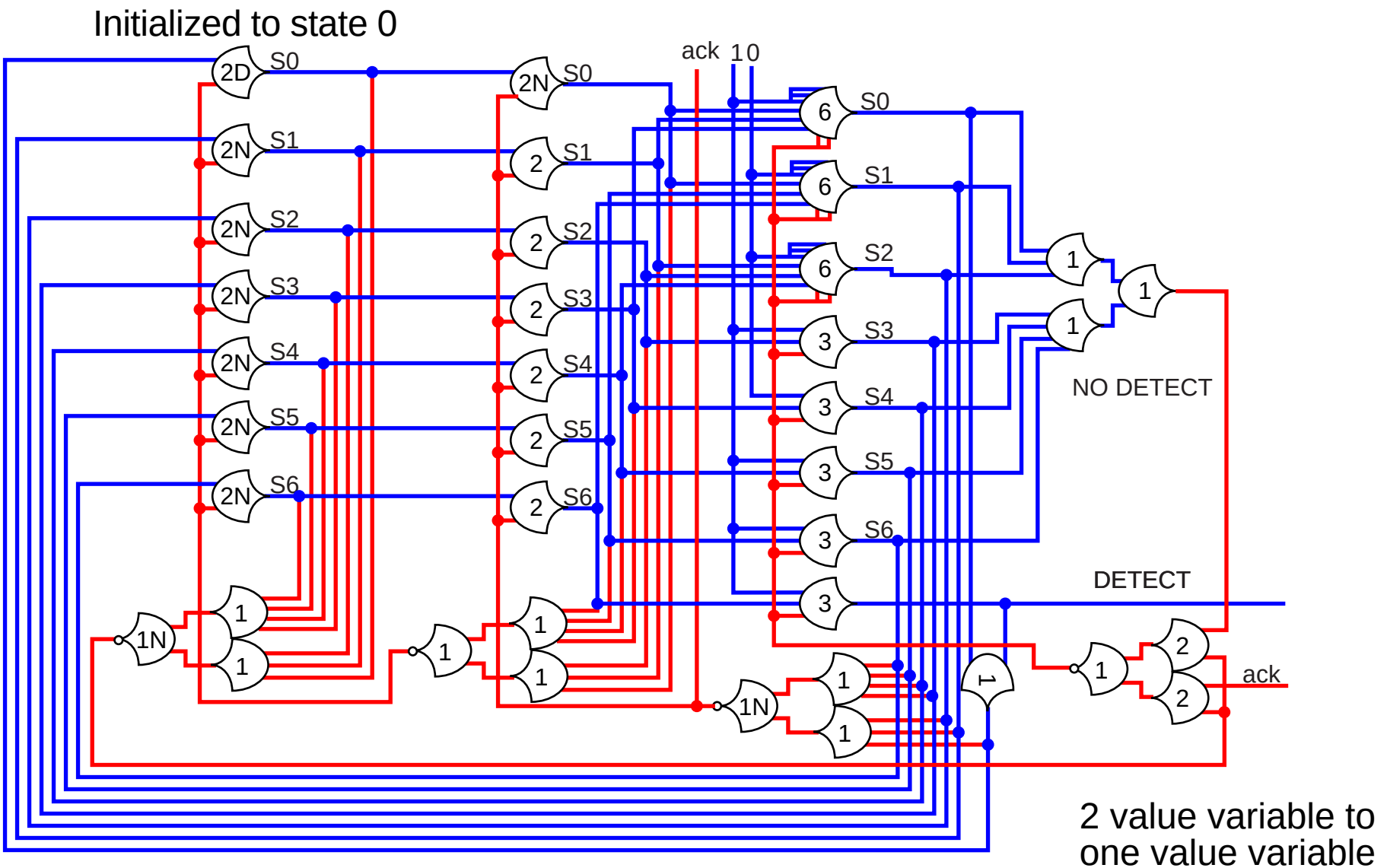
Code Detector State Machine

With intigrated completeness/acknowledge



Code Detector State Machine

Final configuration with 1 value variable output

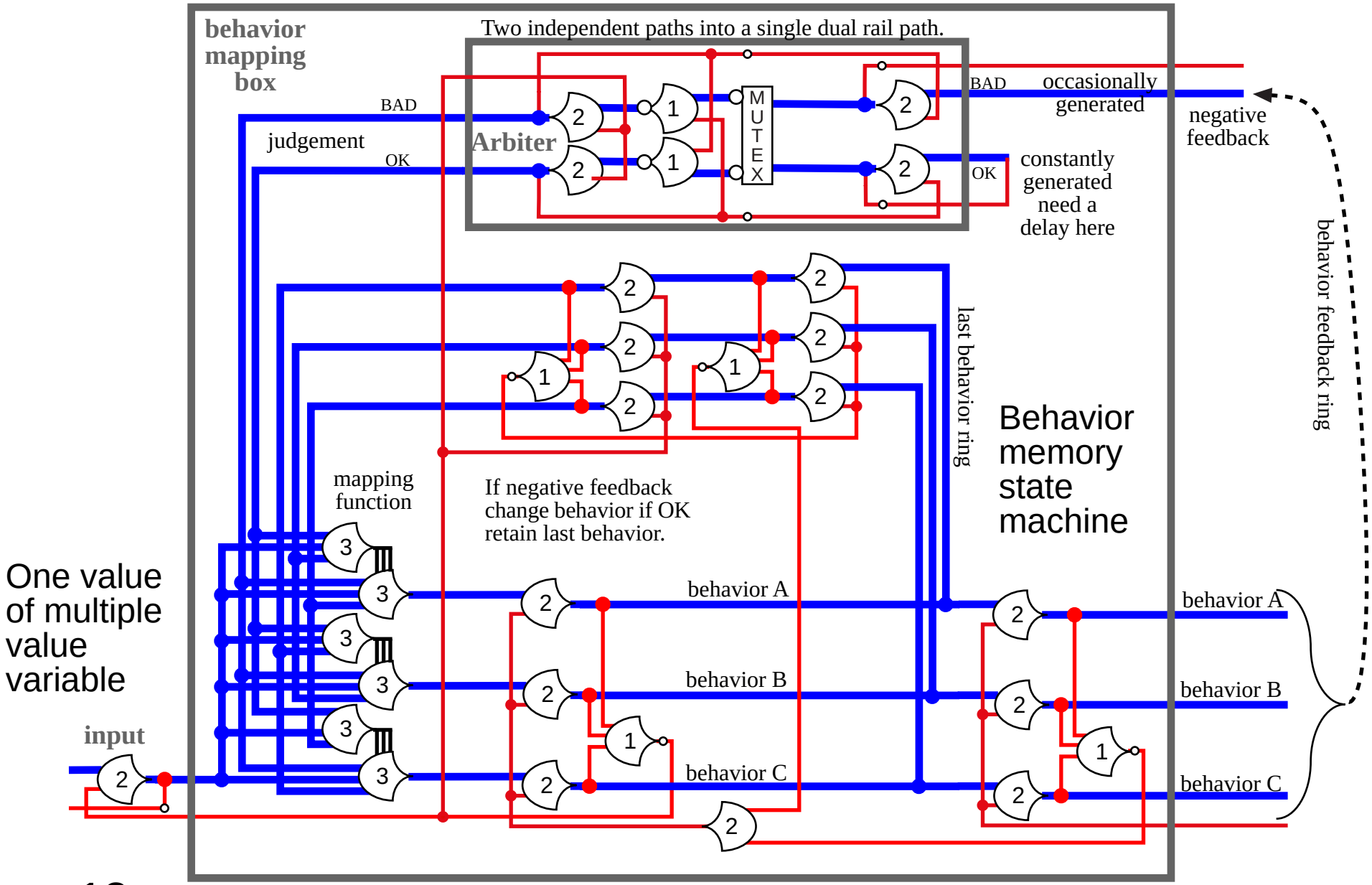


2 value variable to one value variable with auto consume of one value

Embedded Behavior Memory State Machine

From CSR

2 value variable from one value variable with auto produce of one value



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