Presentation Slides

Chapter 6

Memory Elements

Logically Determined Design:
Clockless System Design With NULL Convention Logic

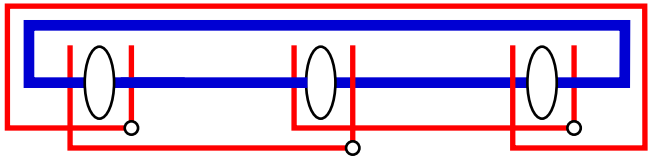
by Karl Fant

John Wiley & Sons, Inc.

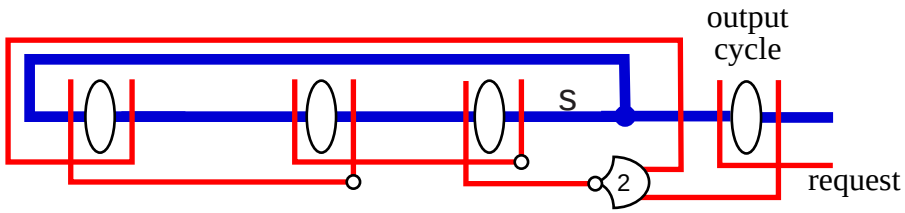
NCL memory structures

Constructing a Memory Ring 1

Three cycle ring

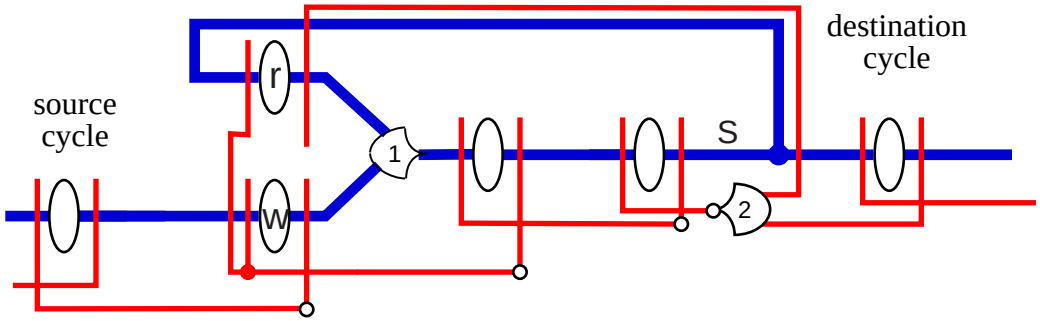


Will remember an initialized wavefront cycling forever.



Add a shared output path

The remembered wavefront will wait in cycle S. When a request ack enables the output cycle the wavefront will flow through the output cycle and through the ring back to S.

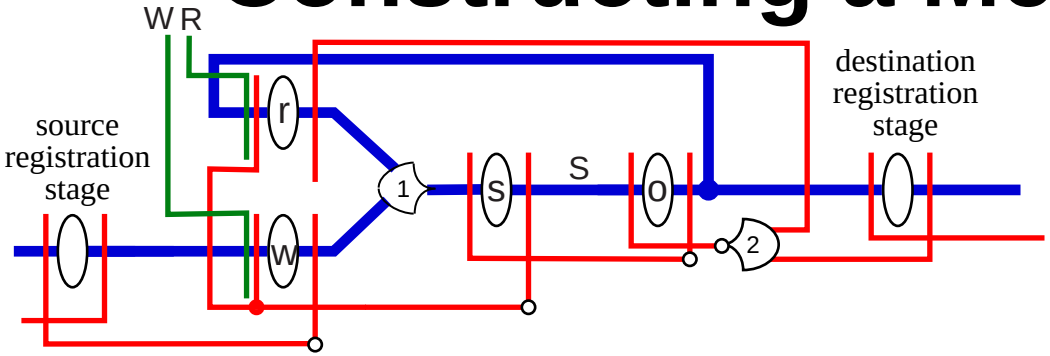


Add a shared input path

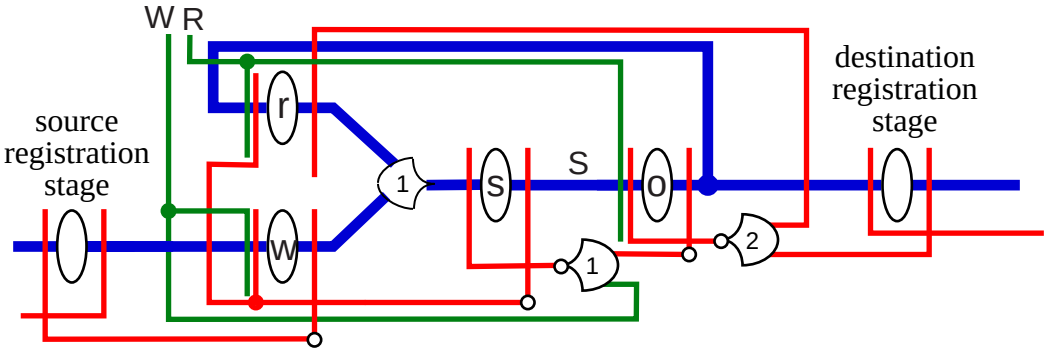
The flow to S can be feedback in the ring or the external input .

The flow from R and W into S can conflict (race). We either have to insure that the R and W wavefront flow is mutually exclusive or we have to arbitrate it.

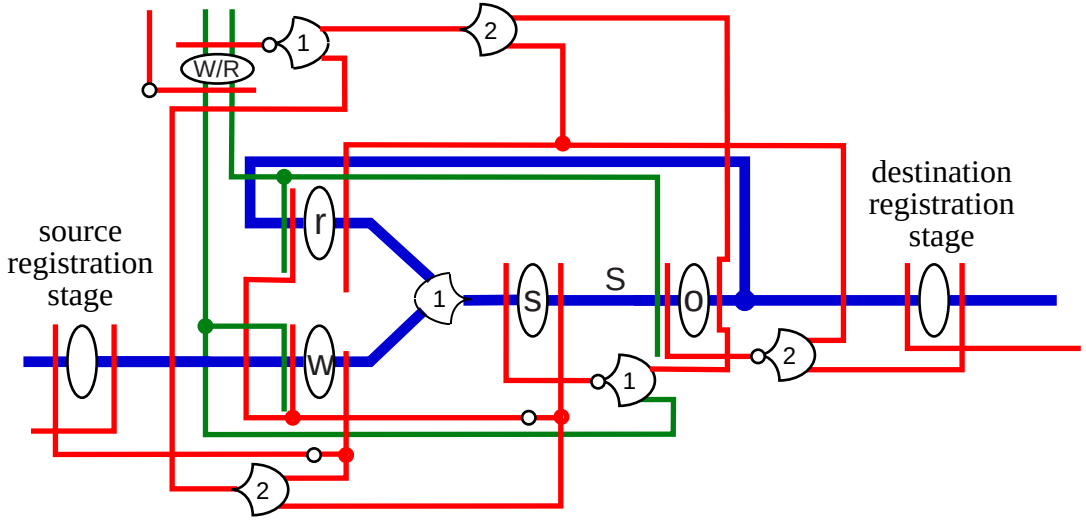
Constructing a Memory Ring 2



A steering variable is added with the values Write (W) and Read (R) which makes the steering values R and W mutually exclusive



The steering variable is extended to steer S to the output or to sink it.



Acknowledge structures are added to close the cycles of the steering variable pipeline

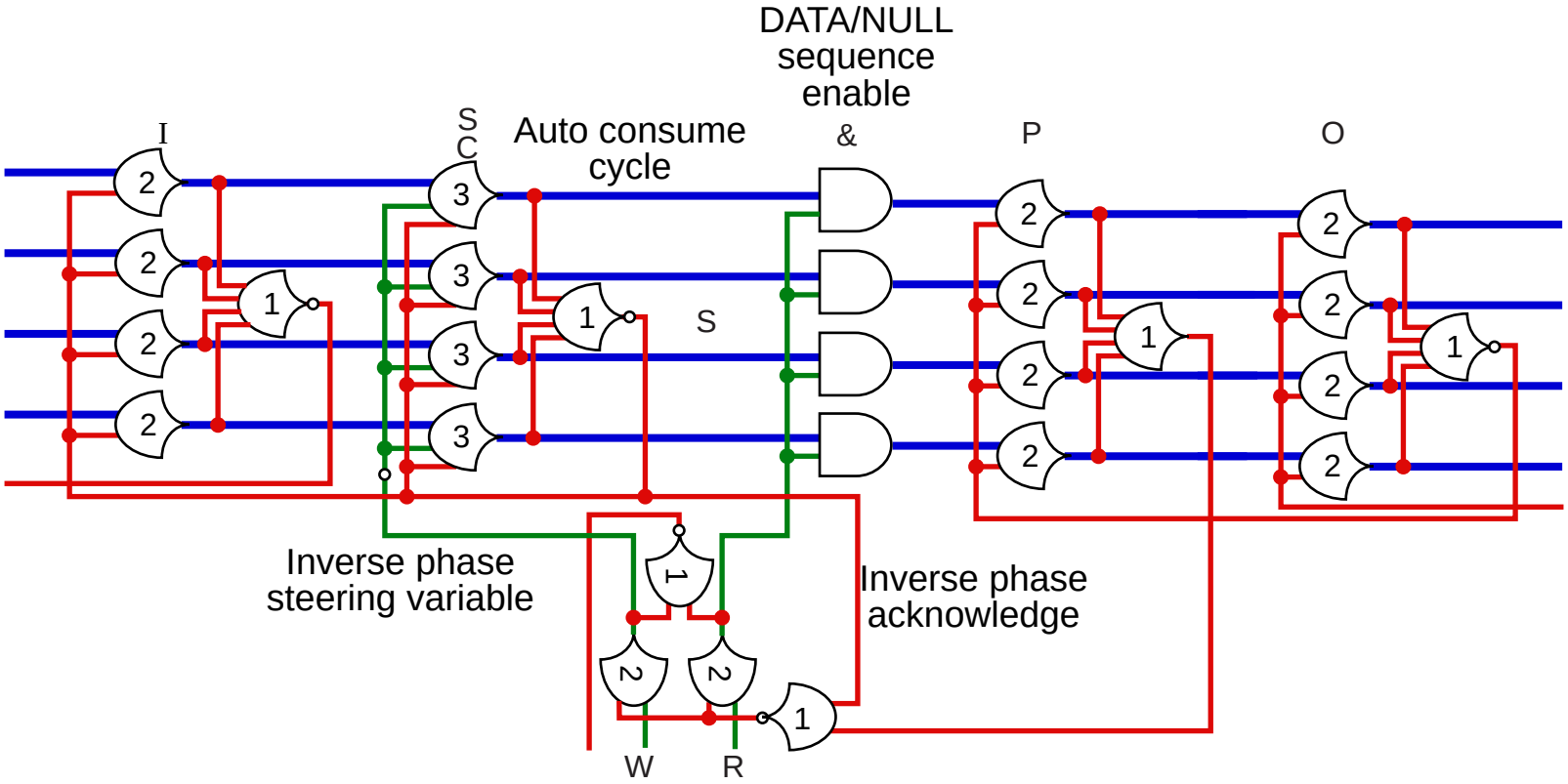
Read: allow wavefront at S to output and to cycle back to S

Write: sink wavefront at S to allow incoming wavefront into S

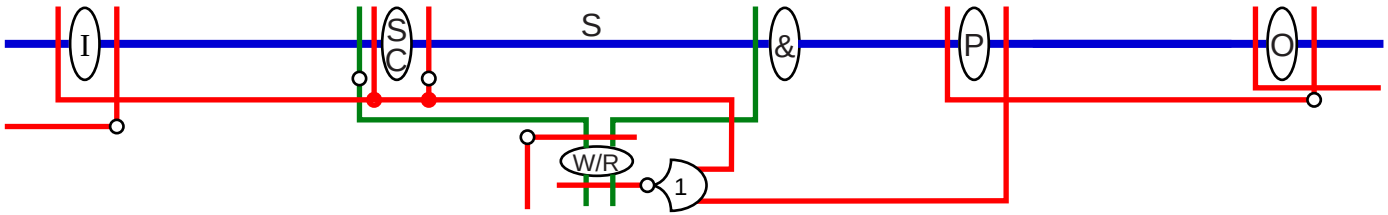
Pipeline Memory

Consume/Produce Register

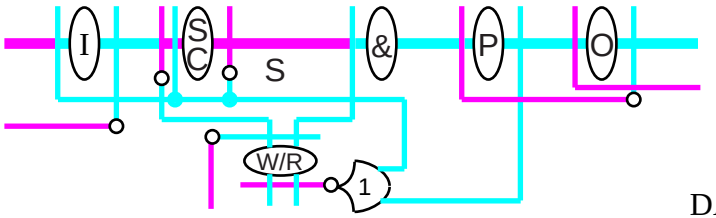
Stop the wavefront in the pipeline and sample it as desired with a rank of AND gates. Functionally identical to memory ring. Faster, smaller, less power.



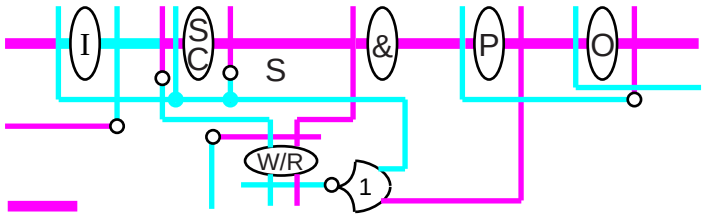
Graphic representation of produce/consume register



Pipeline Memory Read Behavior



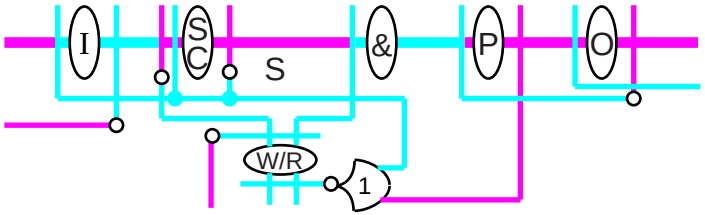
a. Stable waiting for control value



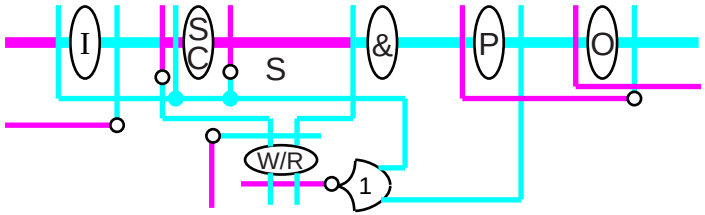
b. Read control value arrives and DATA wavefront is produced

DATA

NULL

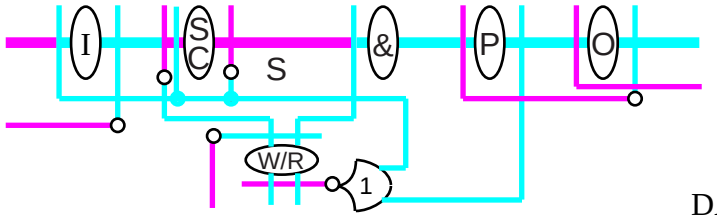


c. NULL control value arrives and NULL wavefront is produced



d. NULL wavefront flows and the register becomes stable waiting for control value

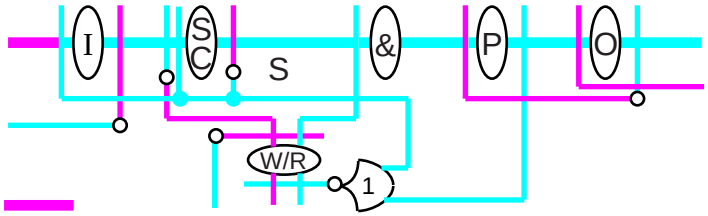
Pipeline Memory Write Behavior



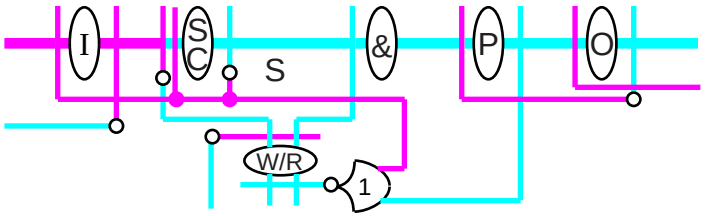
a. Stable waiting for control value

DATA

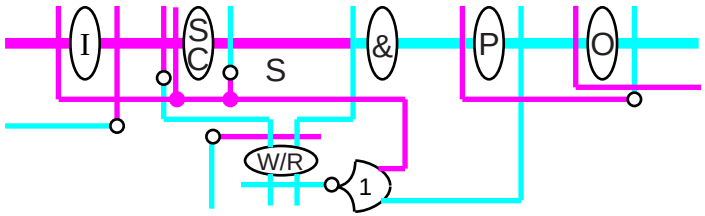
NULL



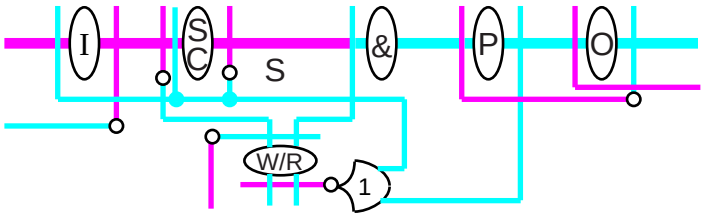
b. Write control value arrives and stored wavefront is consumed



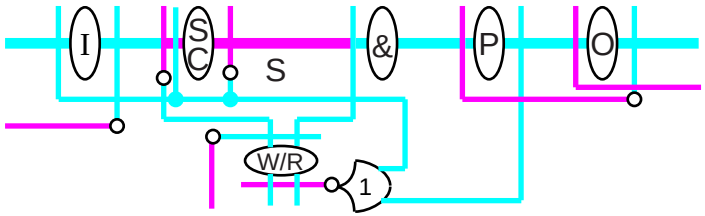
c. The NULL wavefront is detected and DATA is requested from stage I, SC itself and NULL is requested from the control stage.



d. The DATA wavefront flows through the SC stage.

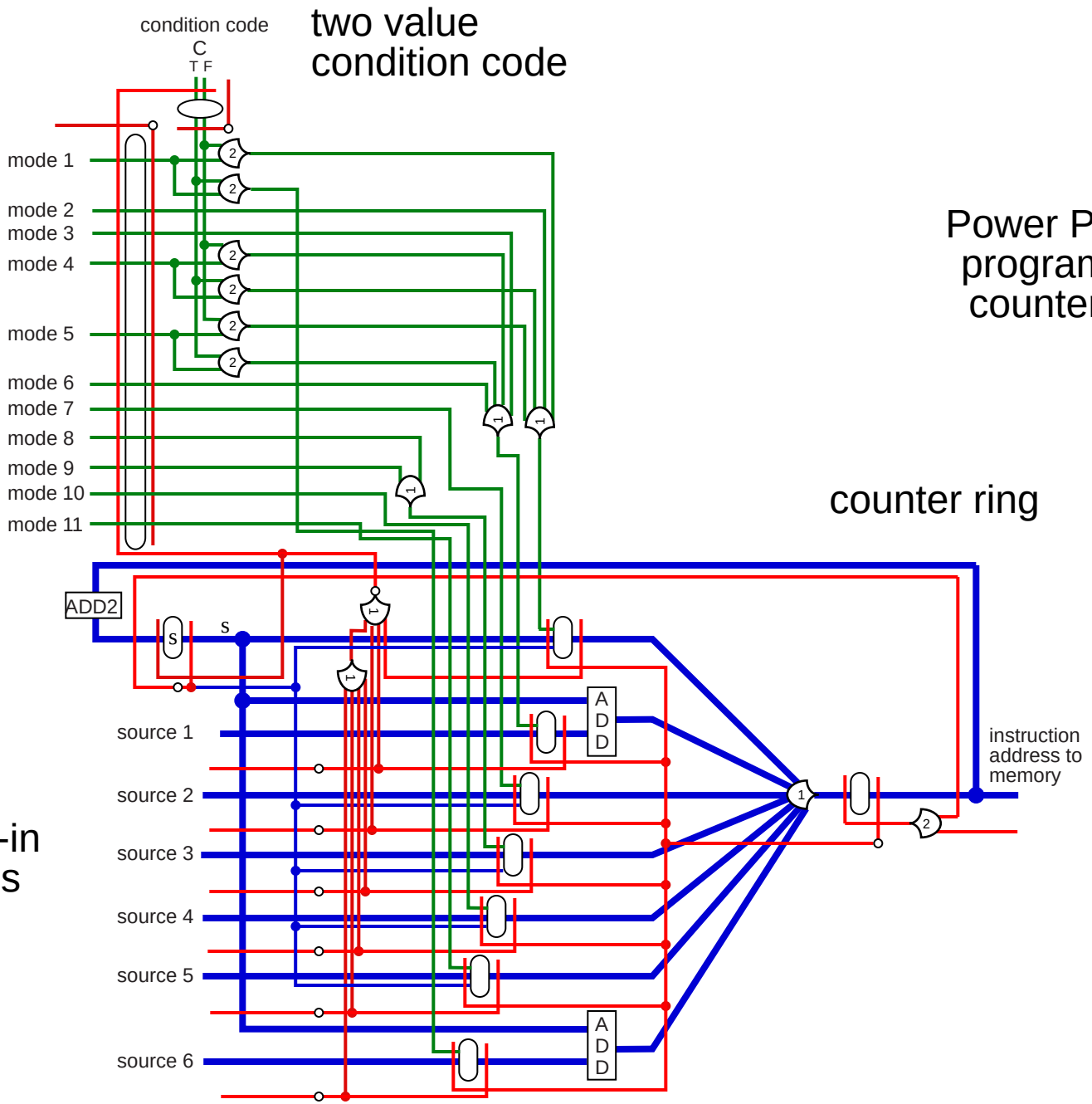


e. The DATA wavefront is detected and NULL is requested from stage I, SC itself and DATA is requested from the control stage.



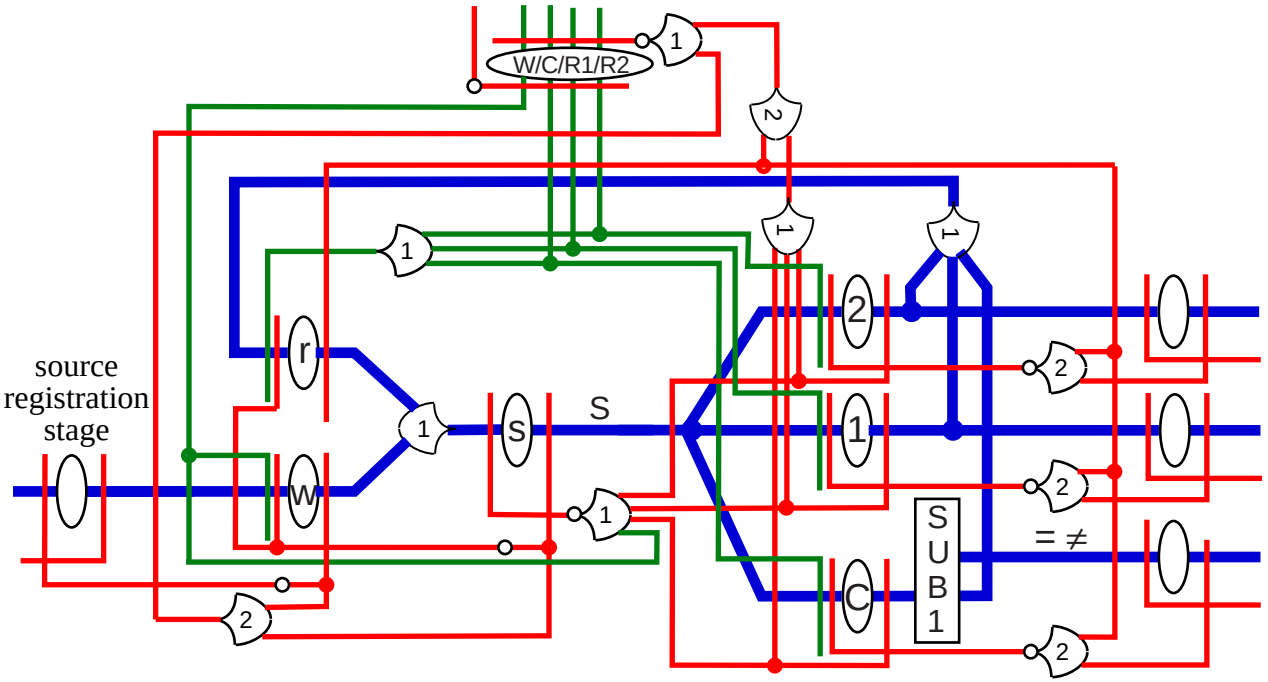
f. NULL wavefront arrives and the register is stable waiting for a control value

Program Counter Register



Counter Register

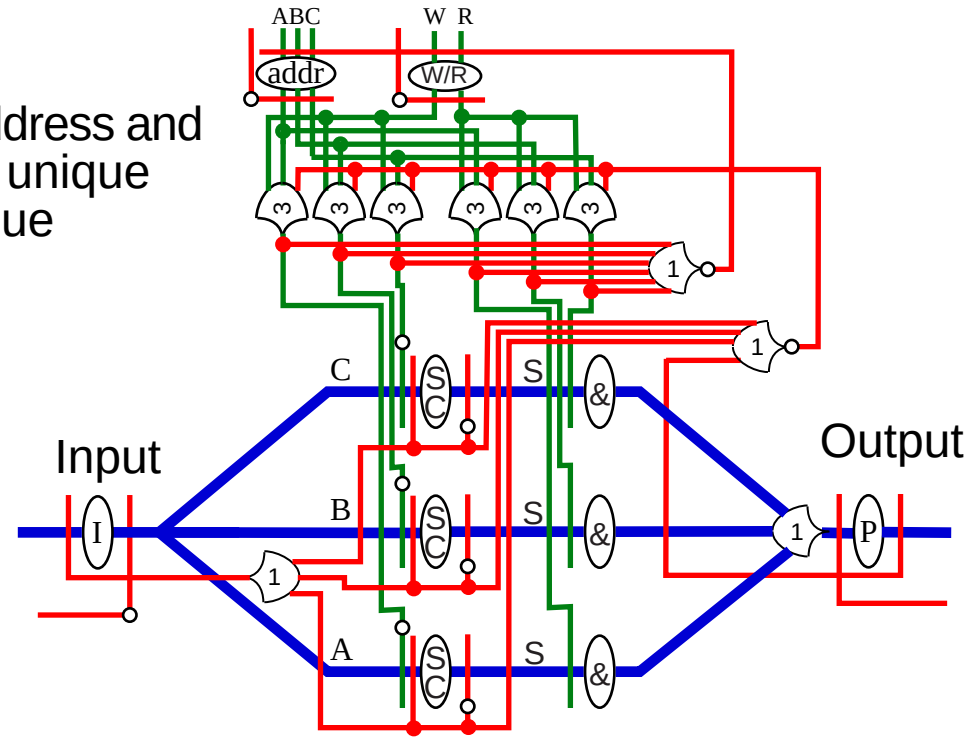
Power PC
counter register



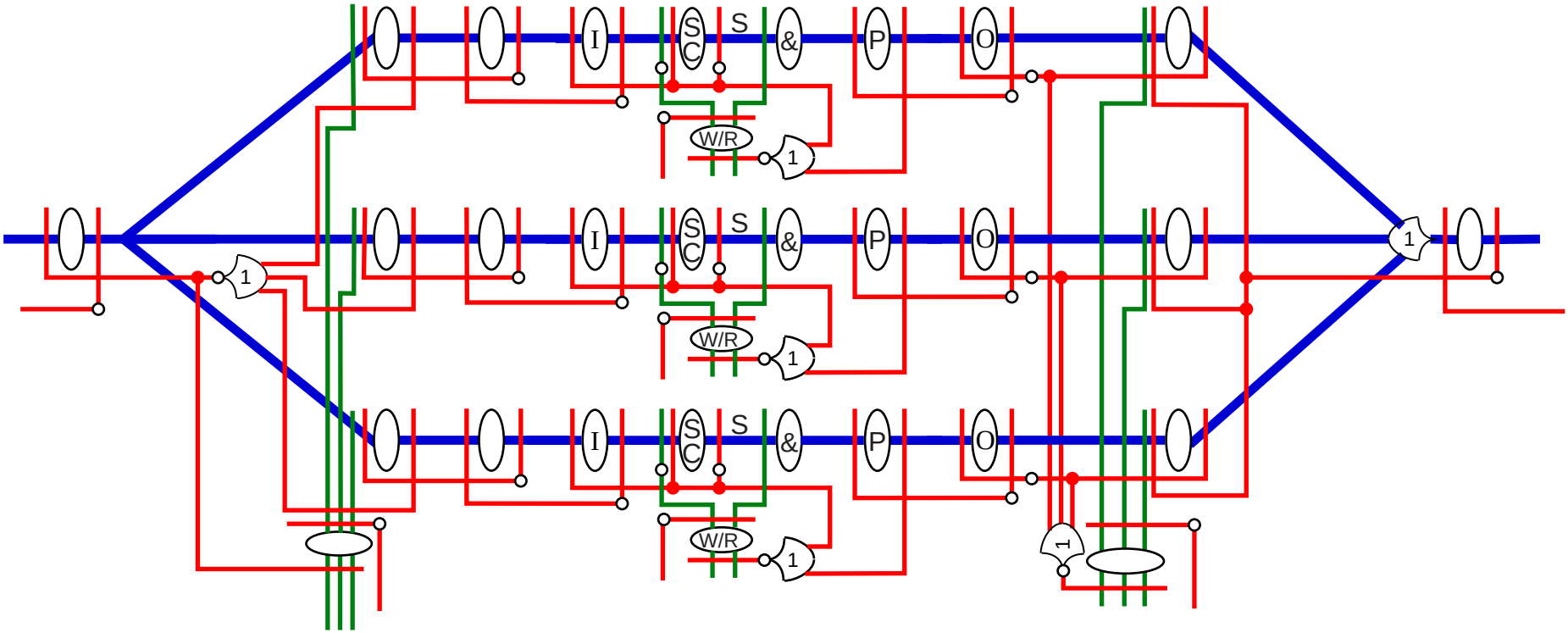
Serial Access Register File

Three location structure. Each location can be individually addressed and written or read.

Combine address and control to a unique steering value



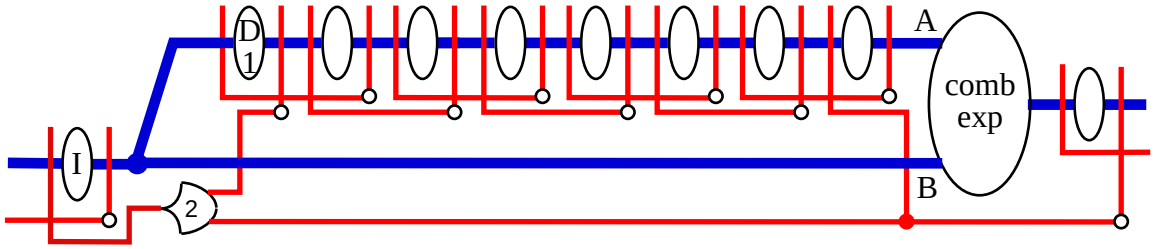
Concurent Access Register File



Delay Pipeline Memory

A wavefront may be delayed M wavefronts in relation to itself through a parallel pipeline in which M wavefronts were initialized.

For each wavefront through the structure one wavefront enters the upper pipeline and one wavefront leaves the upper pipeline.



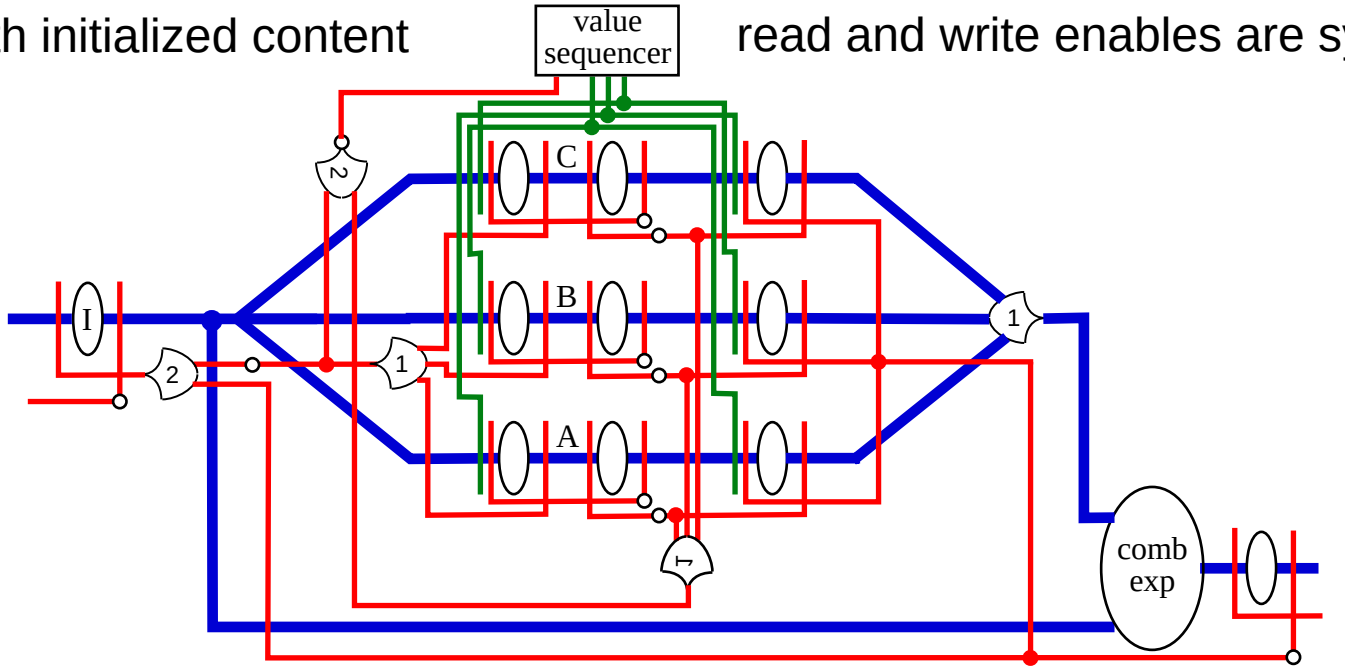
A wavefront enters the structure through I and is fanned out to the upper pipeline and the lower pipeline.

For each Nth wavefront through the structure the Nth wavefront is presented at input B and the (N-M)th wavefront is presented at input A.

Delay FIFO MEmory

Less power and less latency than a pipeline

starts with initialized content

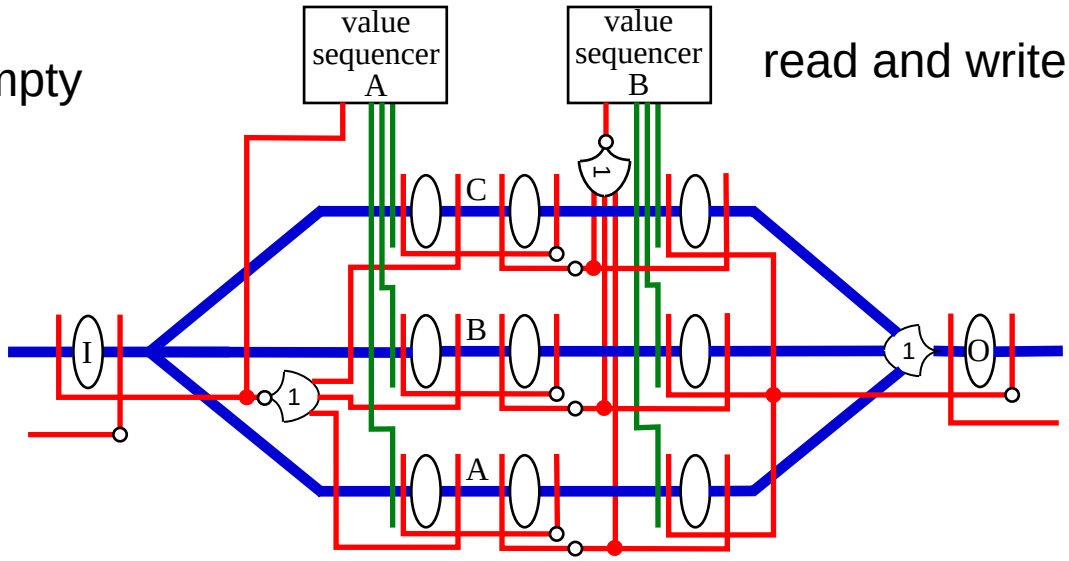


read and write enables are synchronized

FIFO Memory

Write once/read once memory structure
Elastic, variable population memory
The structure can fill up and empty
Read and write bandwidths average out

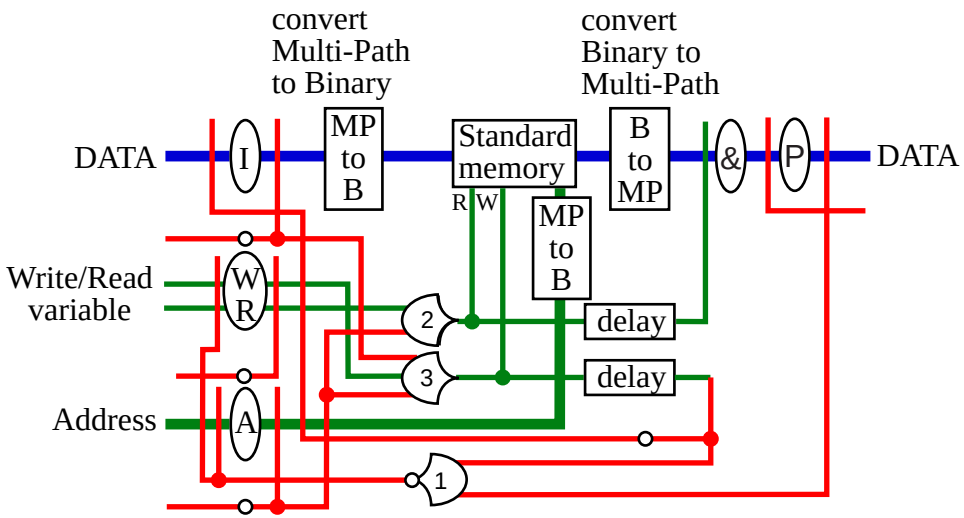
starts empty



read and write enables are independent

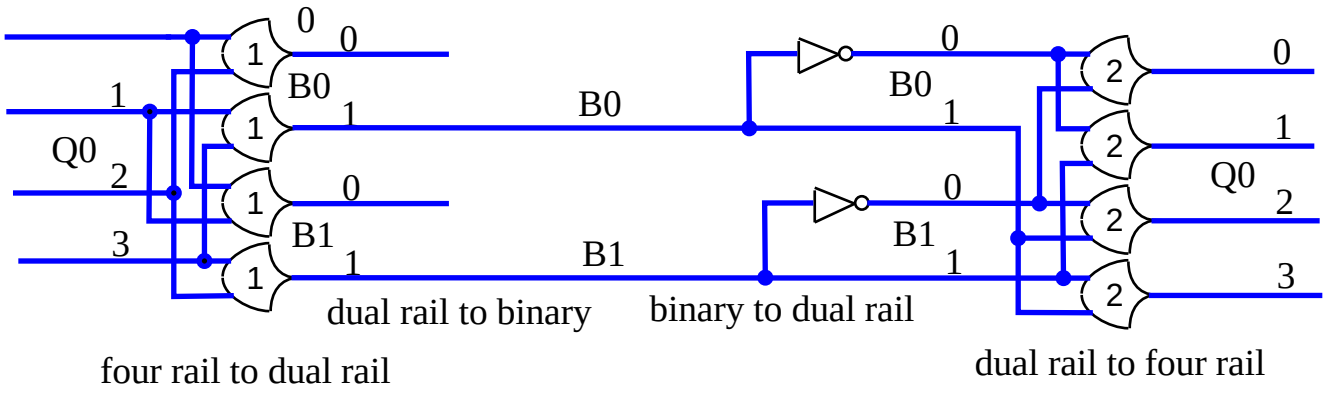
NCL Wrapper for Standard Memory Modules

A standard memory can be integrated into an NCL system by making the memory look like an NCL cycle.



Encoding Conversions

quaternary -> dual-rail binary -> single-rail binary -> dual-rail binary -> quaternary



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