

Presentation Slides

Chapter 5

Cycle Granularity

Logically Determined Design: Clockless System Design With NULL Convention Logic

by Karl Fant

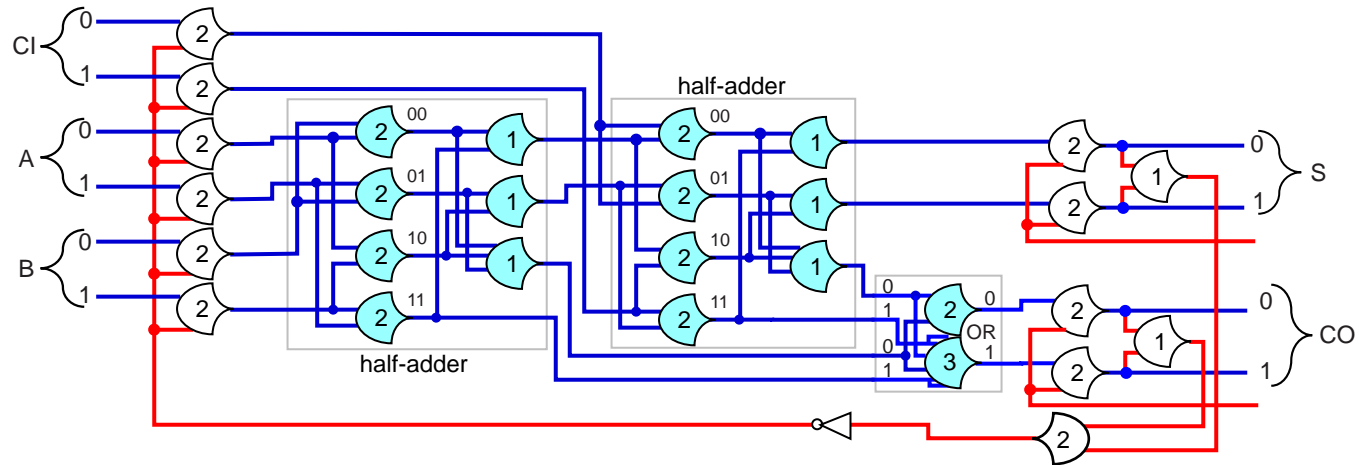
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Introduce cycle granularity and 2D pipelining

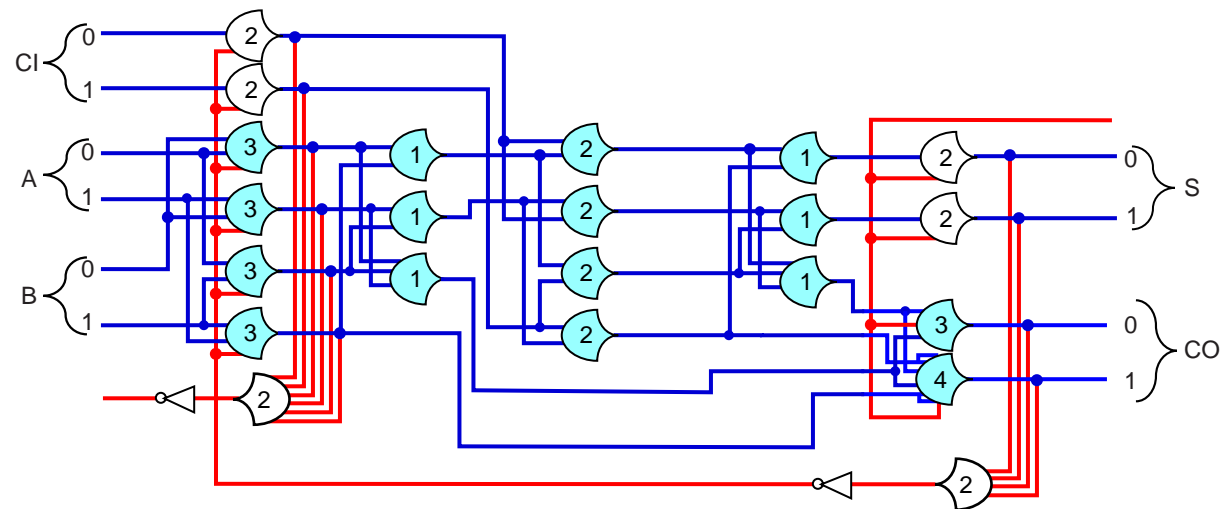
Diagrams by permission of John Wiley & Sons, Inc.

Integrated Coordination

Combinational expression bounded by explicit ranks of logic performing only completeness/acknowledge



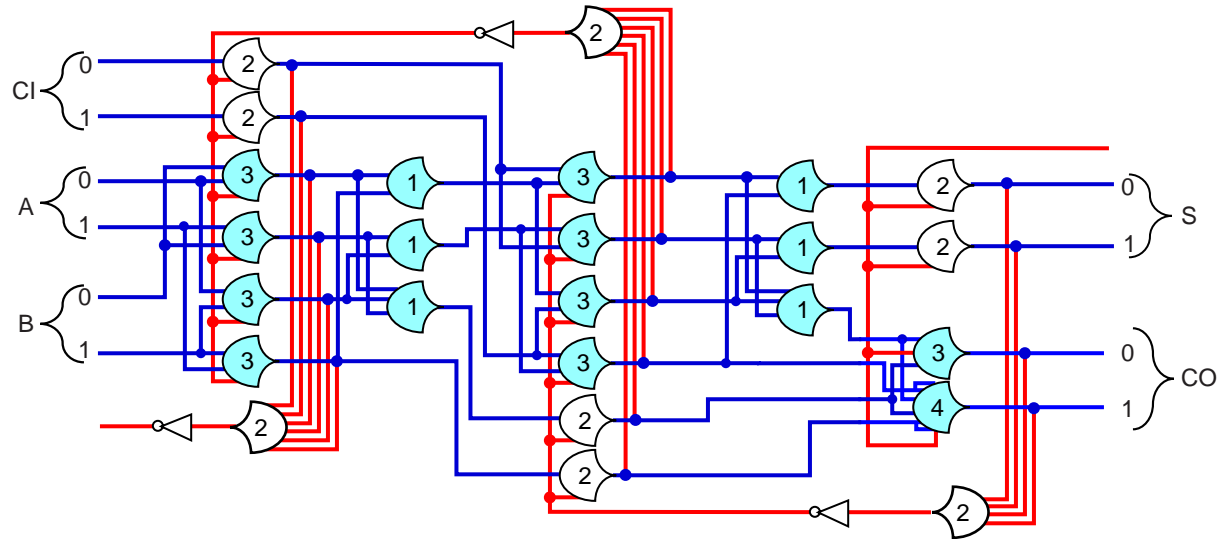
Integrate completeness/acknowledge in first and last ranks of logic



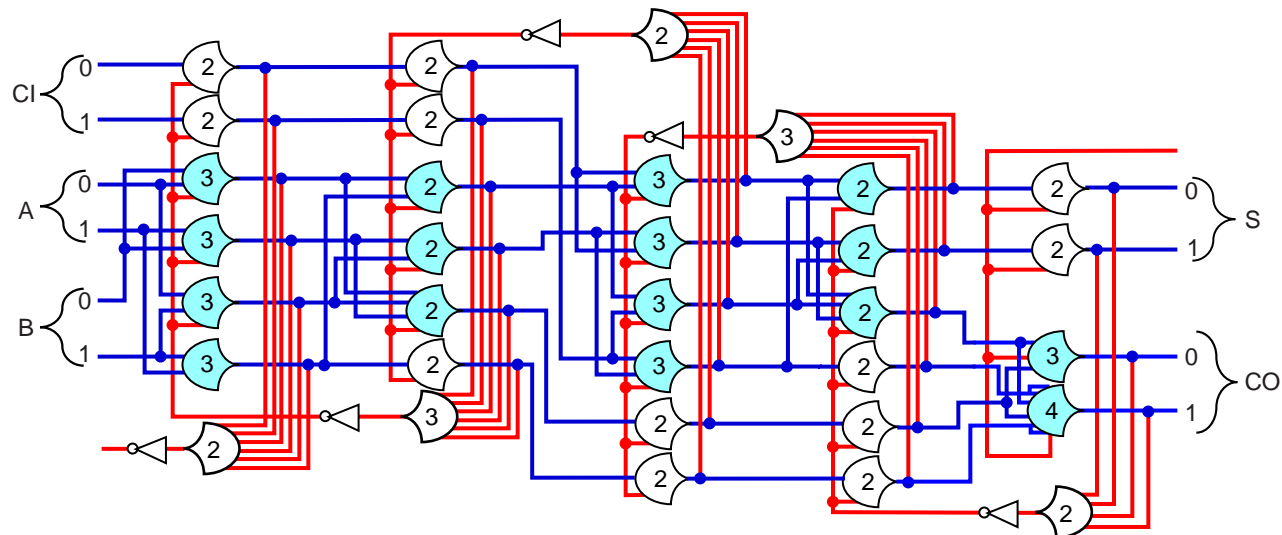
The acknowledge regulation behavior is integrated into the logic operators. The acknowledge path is added as input and the threshold is increased by 1.

Rank Level Pipelining

Integrate completeness/acknowledge into a middle rank forming a finer grained pipeline



Integrate completeness/acknowledge in every rank of logic

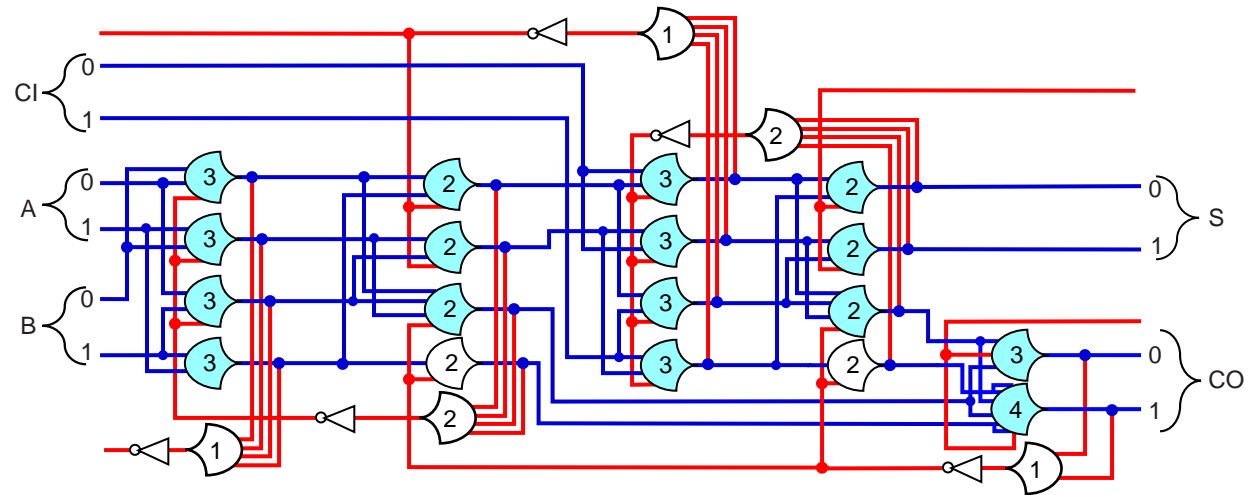


Variable Level Pipelining

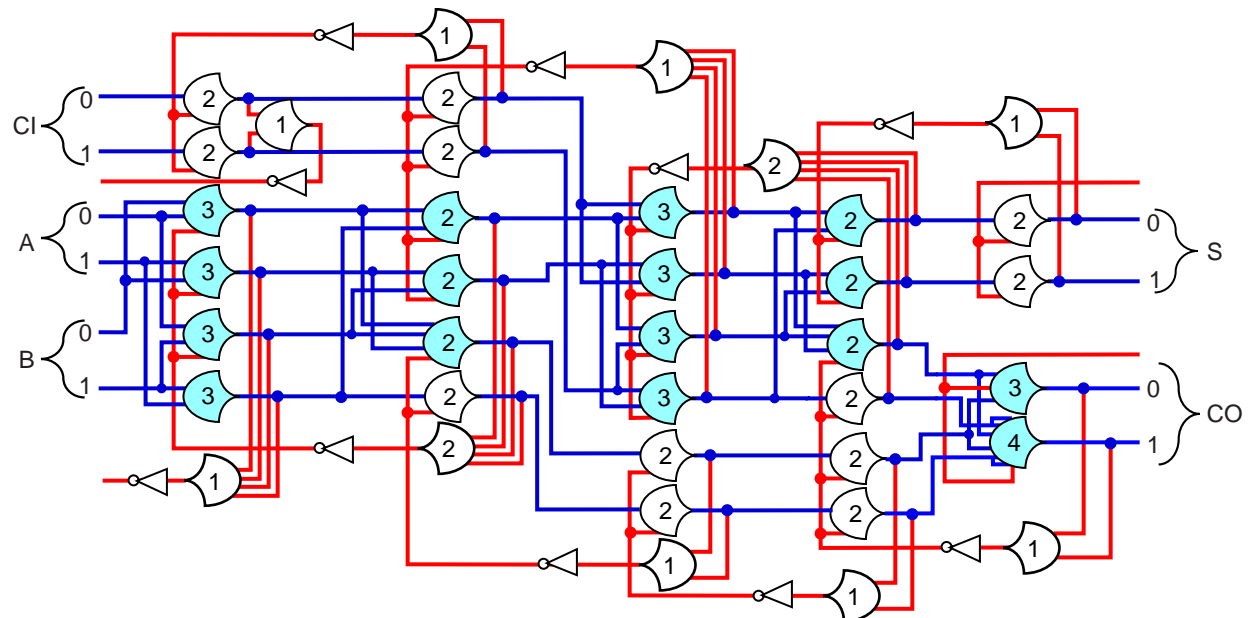
Every variable acknowledges all variables that contribute to it.
Every variable is acknowledged by each variable to which it contributes.

Finest granularity cycle structure

There is no operator performing solely a data function. All operators are contributing to cycle coordination.

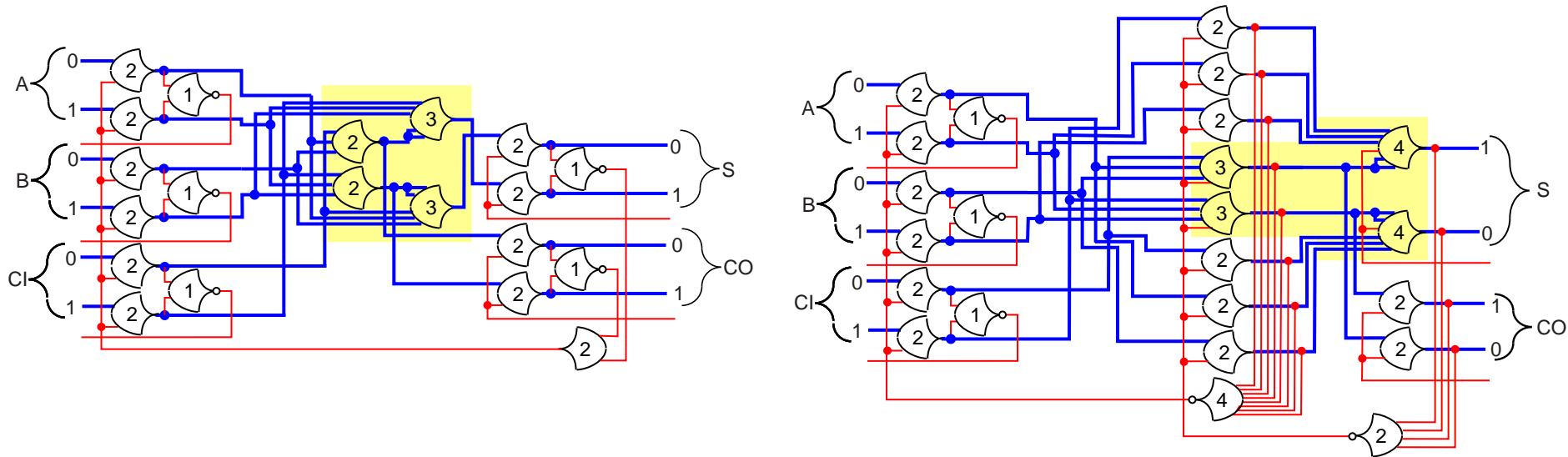


Variable pipelining with cycle buffering insuring shortest cycle periods provides identical functionality just with faster throughput.



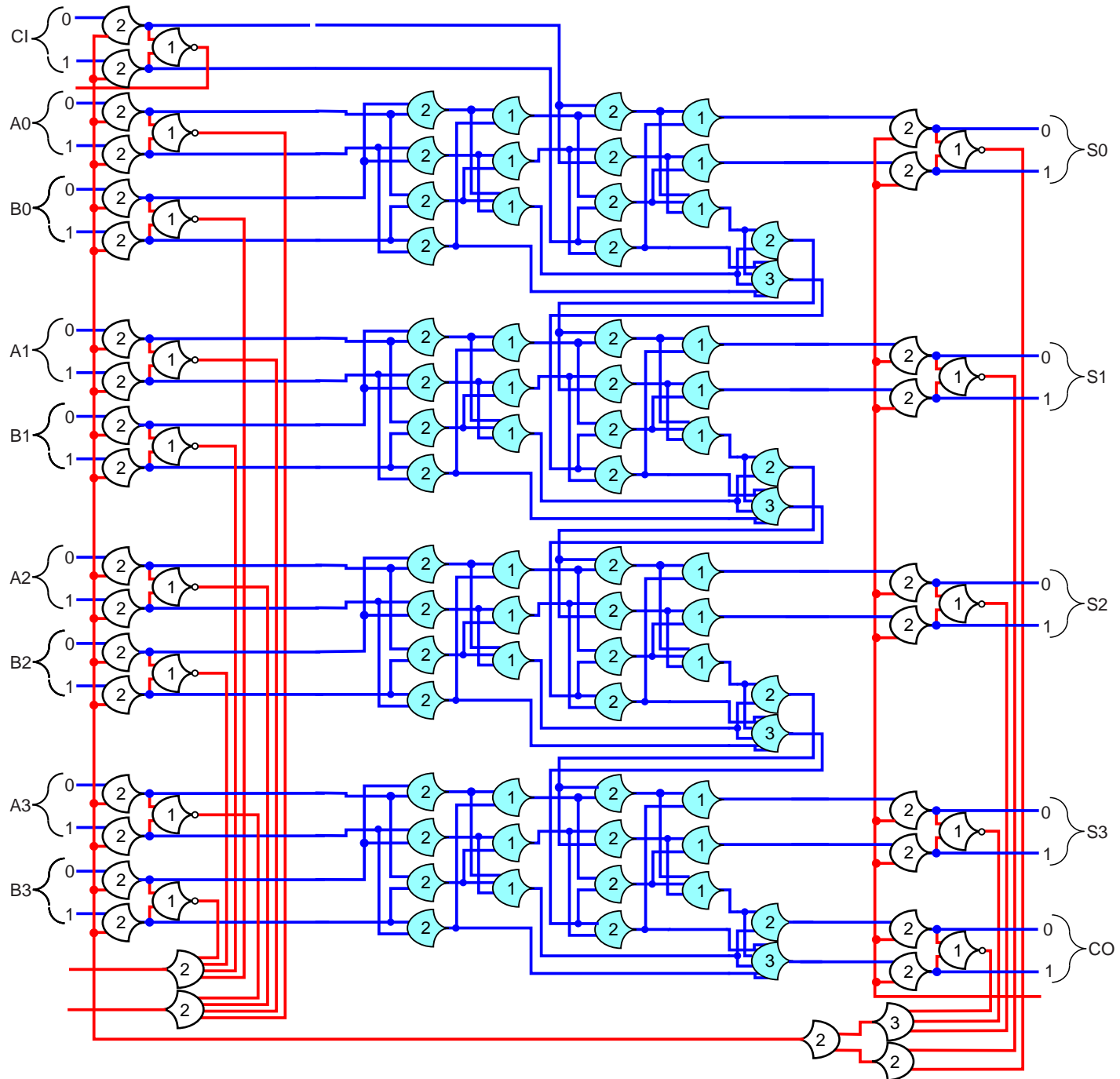
Too Fine Grained Partitioning

It can be expensive to partition too finely. The full adder, for instance, does not have an internal variable boundary and one has to be created to partition between the operators.



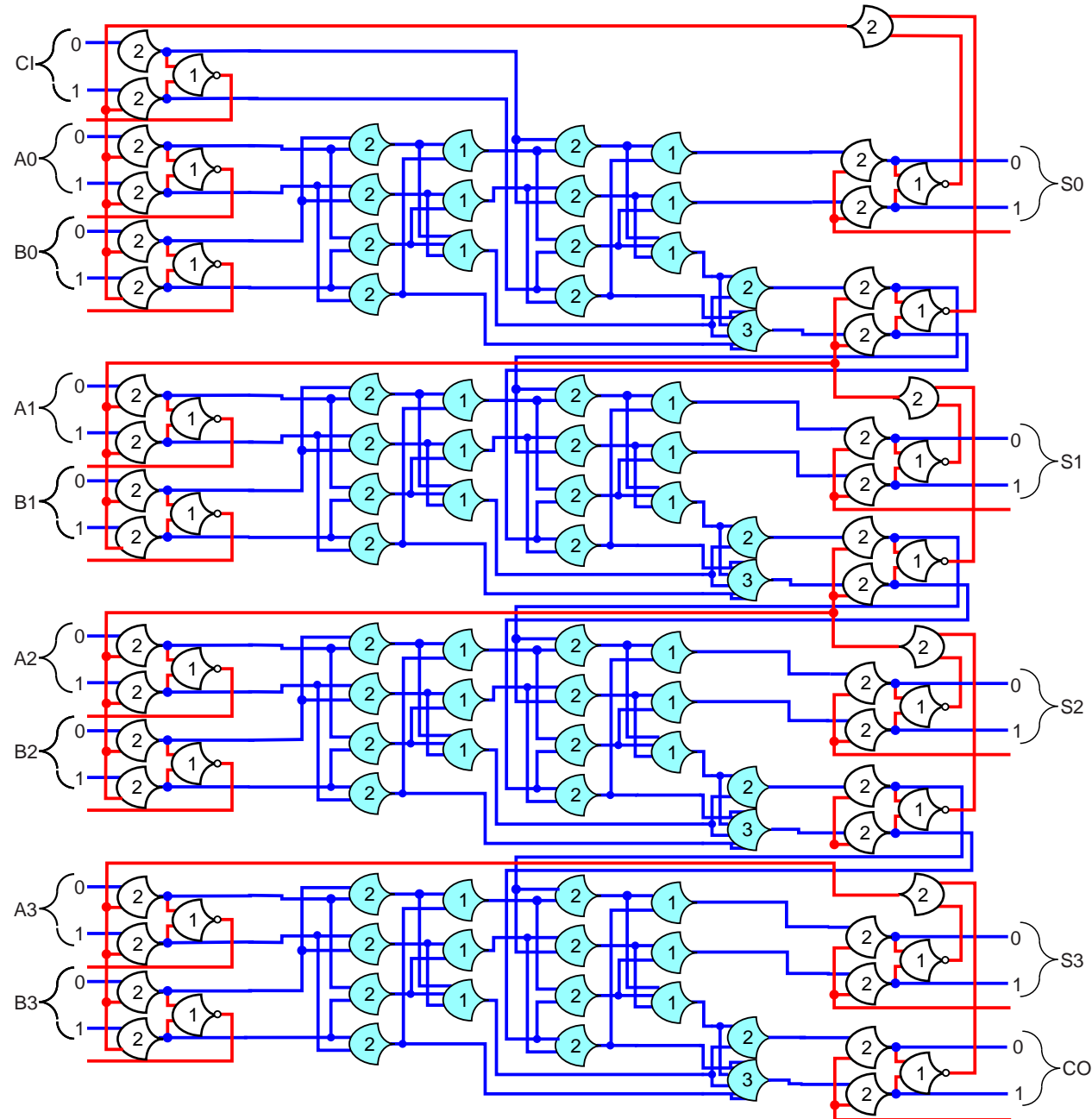
Four Bit Adder

Full Data Path Width Cycle. Explicit Registration.



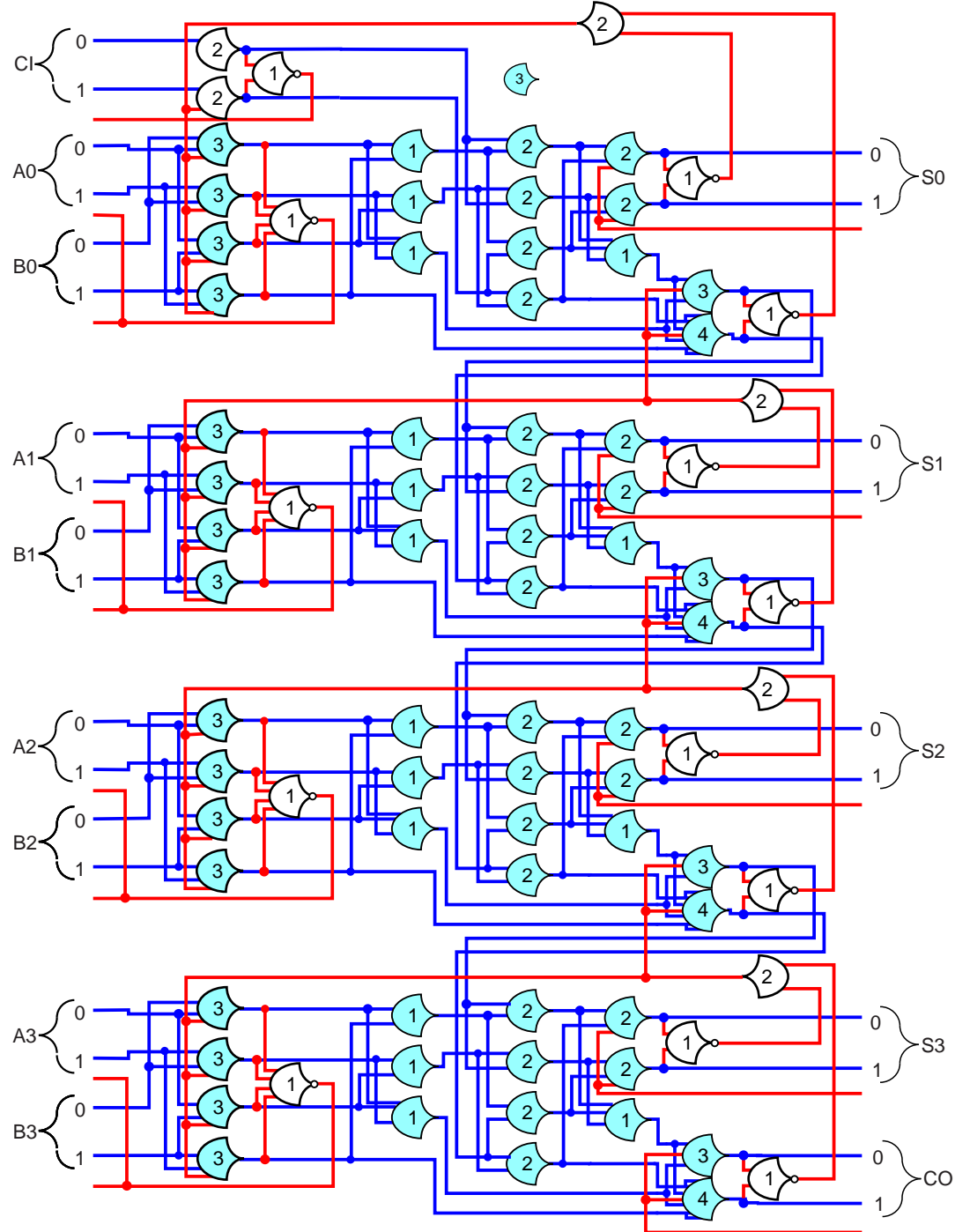
Four Bit Adder

Bit Width Cycles. Explicit Registration.



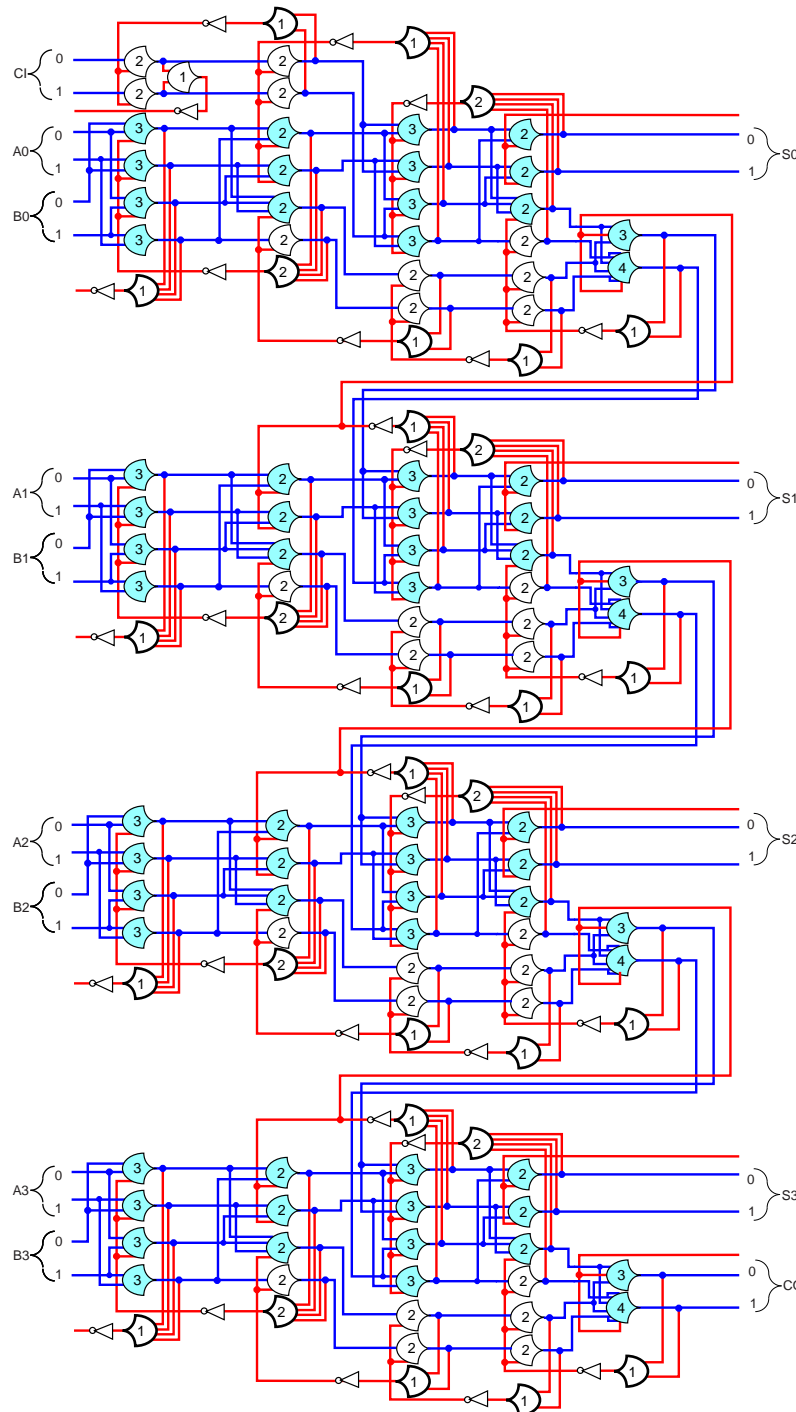
Four Bit Adder

Bit Width Cycles. Integrated Registration.



Four Bit Adder

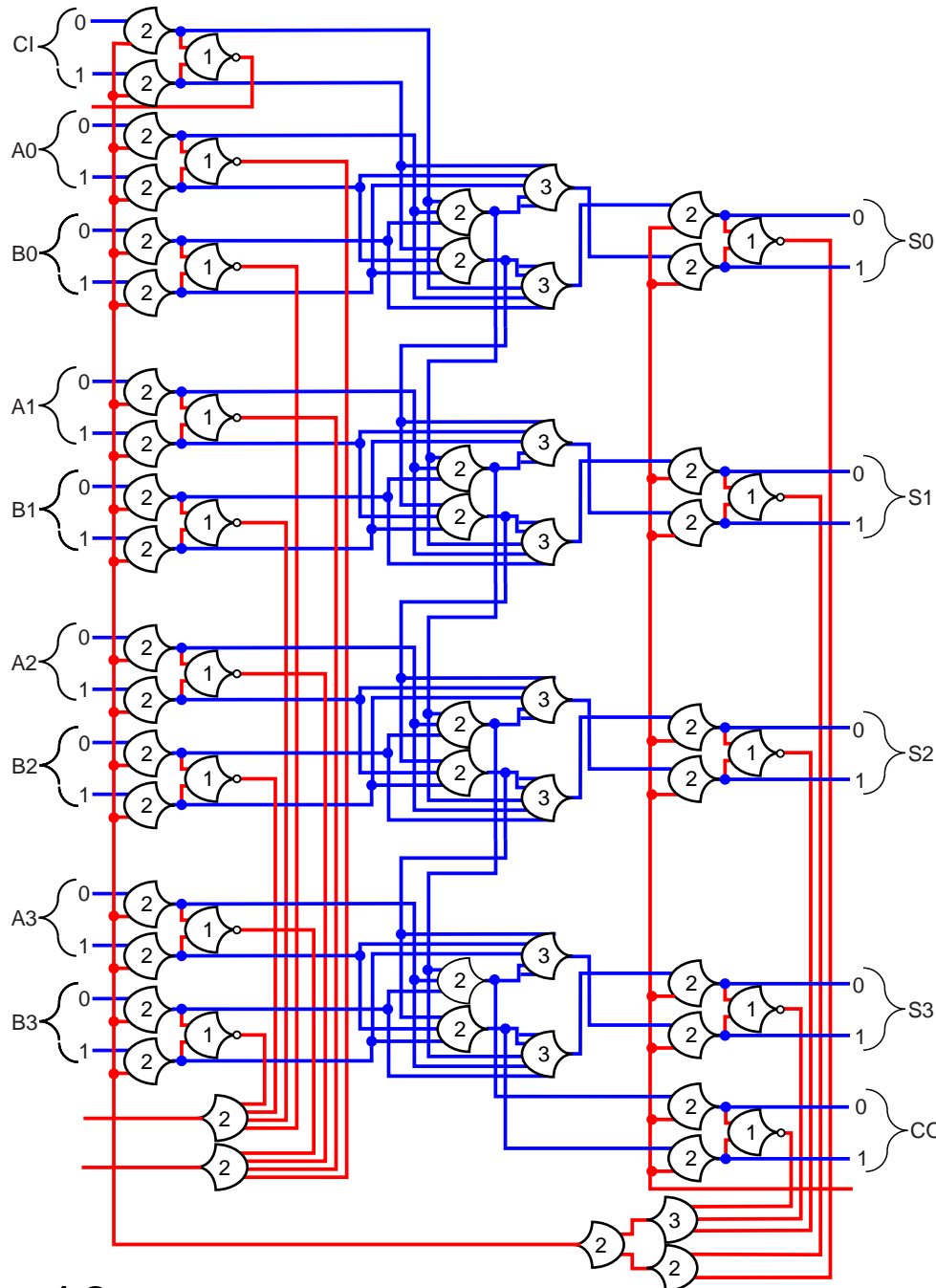
Primitive Level Cycles. Finest Granularity Cycles.



functionally identical to page 6 but with much higher throughput.

Four Bit Adder

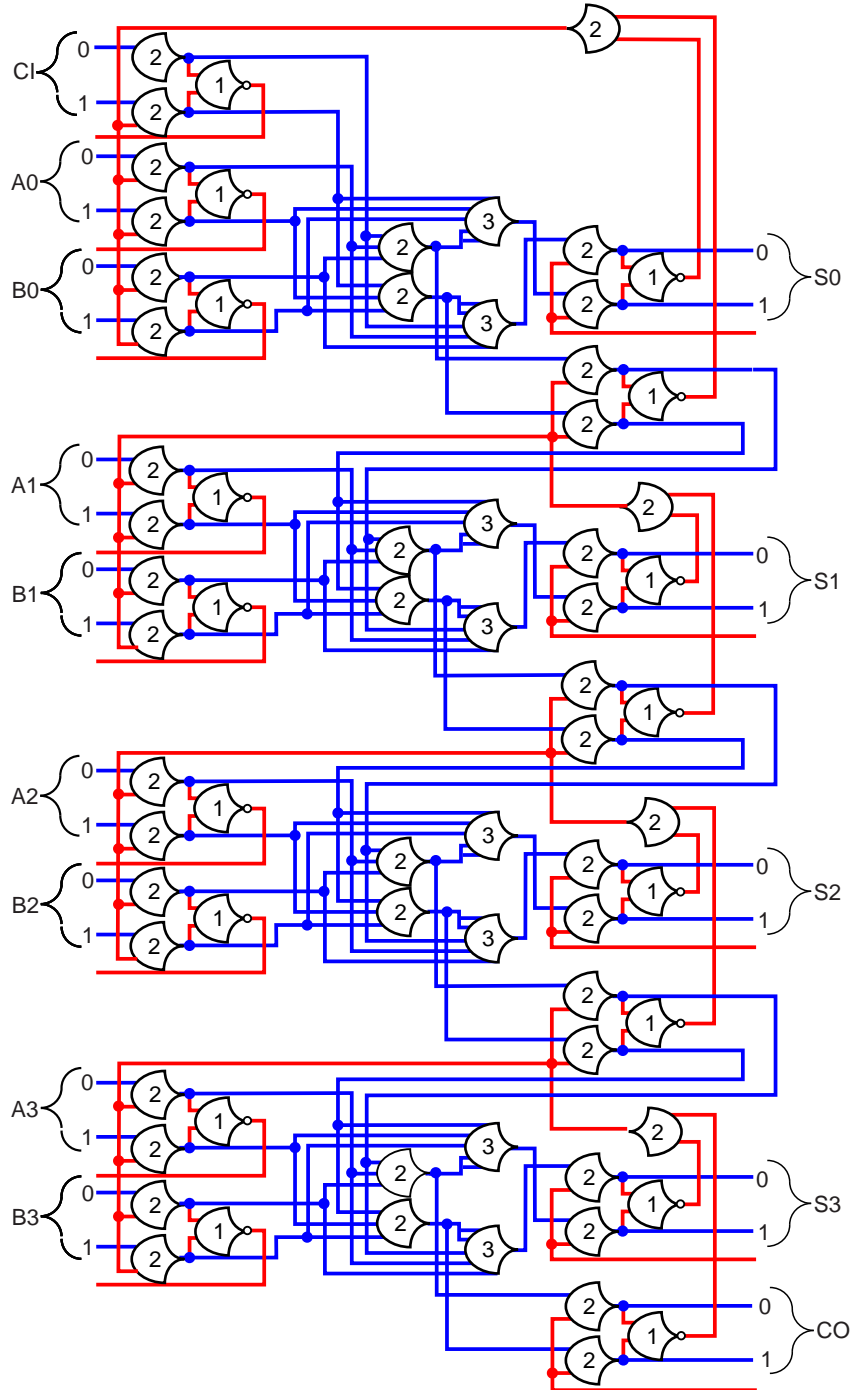
Full Data Path Width Cycle. Explicit Registration.



Using optimal NCL
full adder.

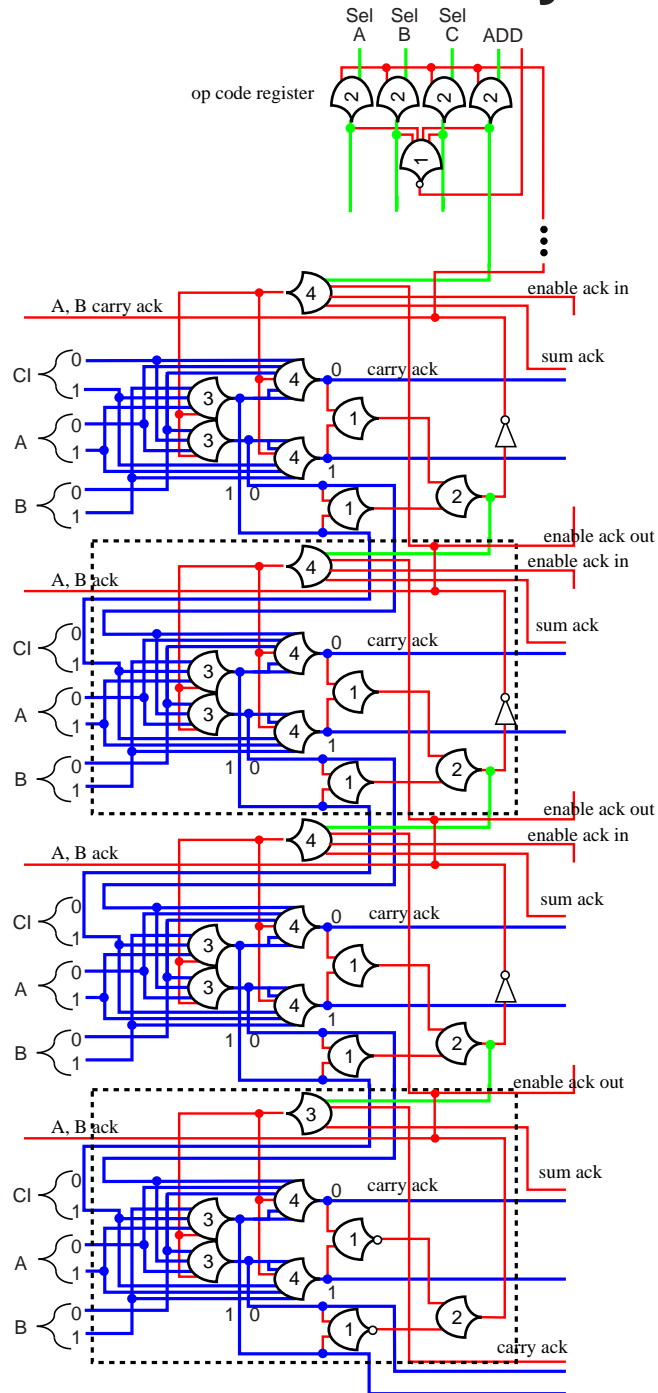
Four Bit Adder

Bit Width Cycles. Explicit Registration.



Four Bit Adder

Bit Width Cycles. Integrated Registration.

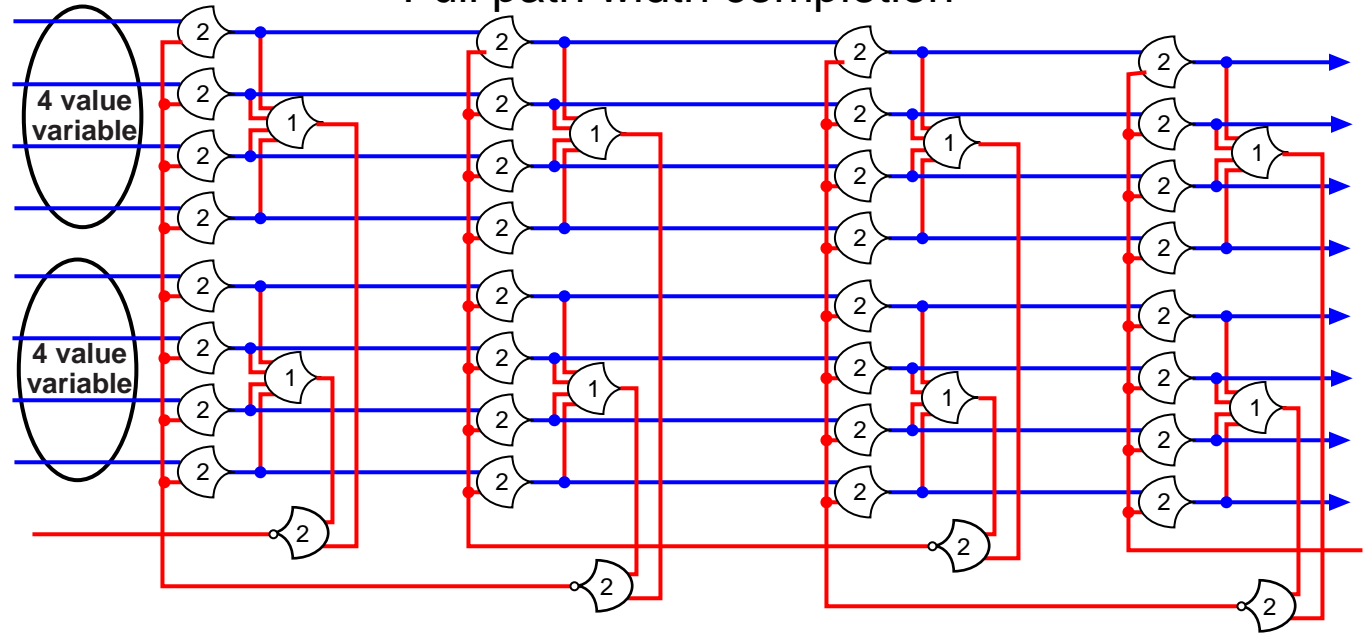


Using optimal NCL
full adder.

also with integrated
steering pipelining
along with CARRY

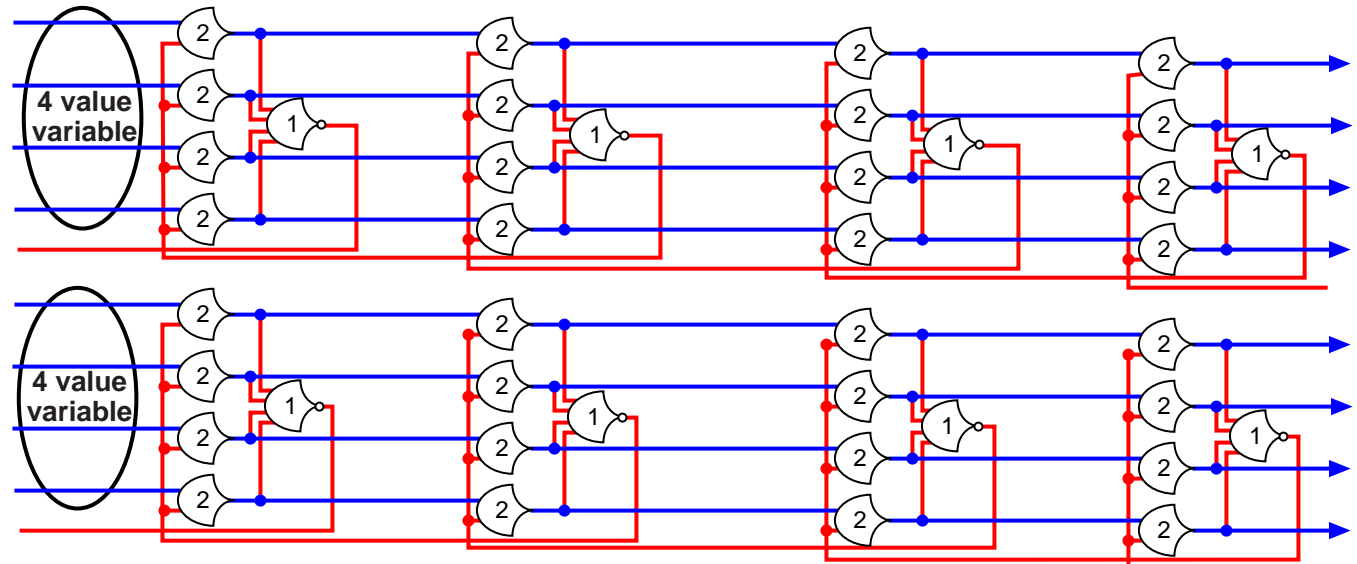
Data Path Variable Partitioning

Full path width completion



Completeness only has to be expressed among genuine dependencies. If there are no dependency relationships then mutual completeness coordination is unnecessary

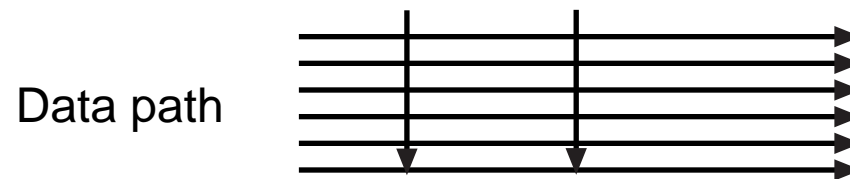
Partitioned path completion. Individual variables can flow freely.



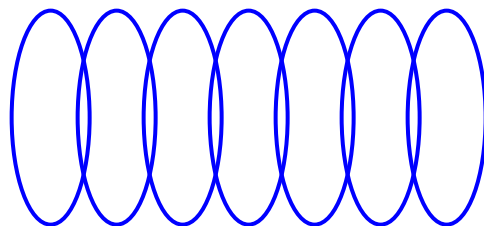
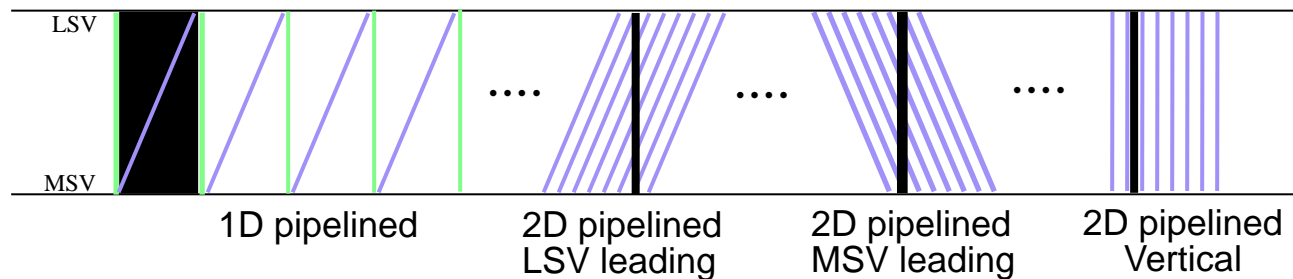
2D Pipelining the Data Path

A DATA path can be partitioned even if there is a dependency relationship among the variables such as the carry dependence or a data path spanning control variable.

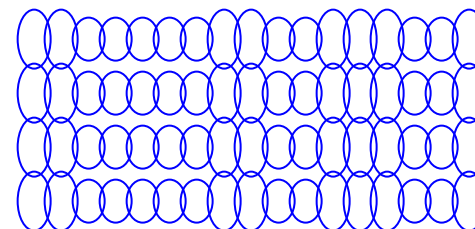
A data path can be viewed as a set of parallel pipelines each carrying one variable. Dependency relationships among the variables can be pipelined orthogonally across the data path



Diagonal Wavefront Flow



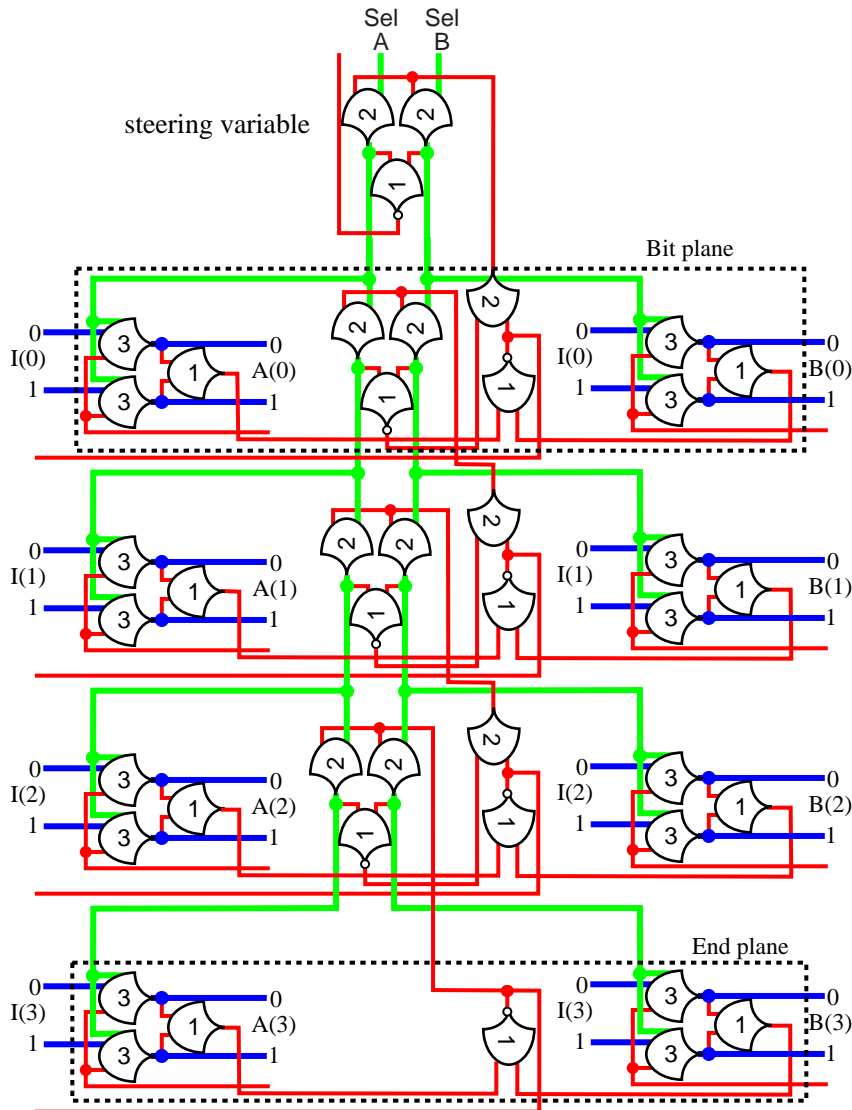
Cycle structure of 1D spanning completeness data path



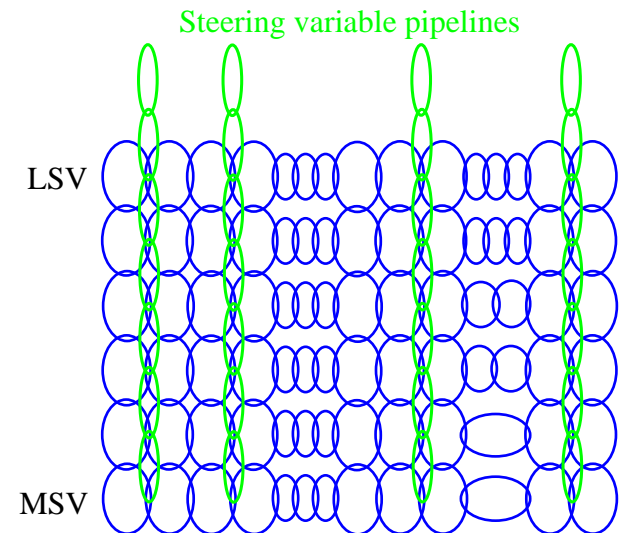
Basic cycle structure of 2D pipelined data path

2D Pipelined Steering Variables

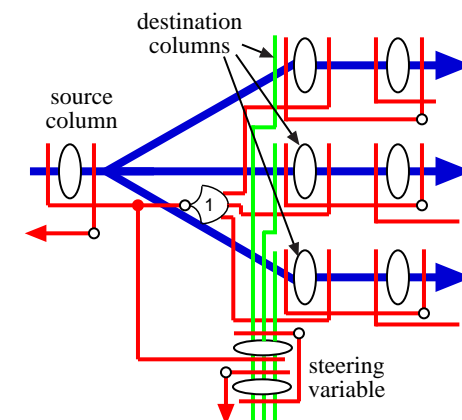
This is a two way fan-out steering structure that steers from a common source column $I(n)$ to destination column $A(n)$ or $B(n)$.



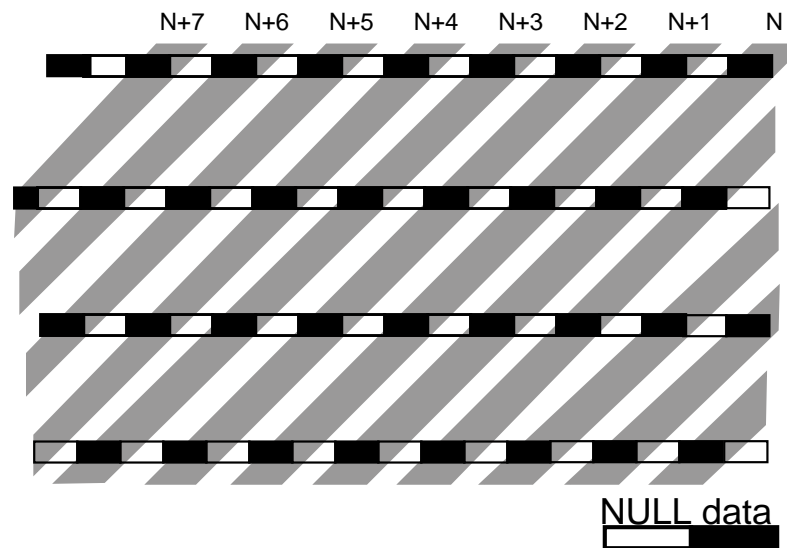
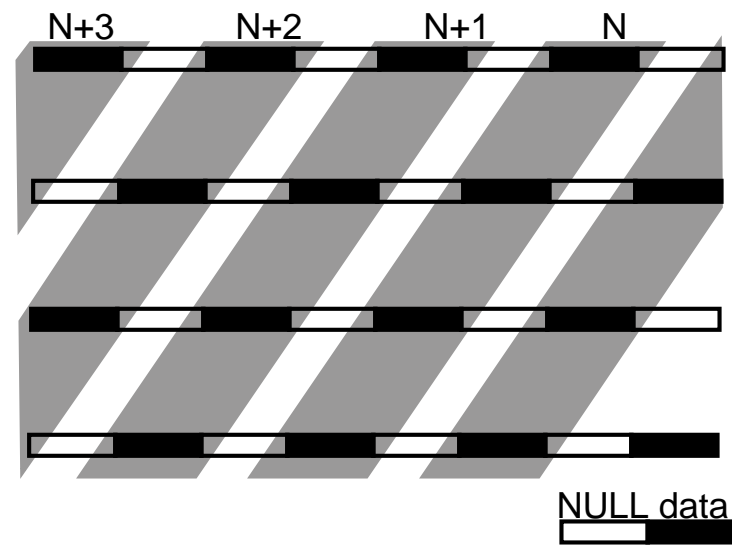
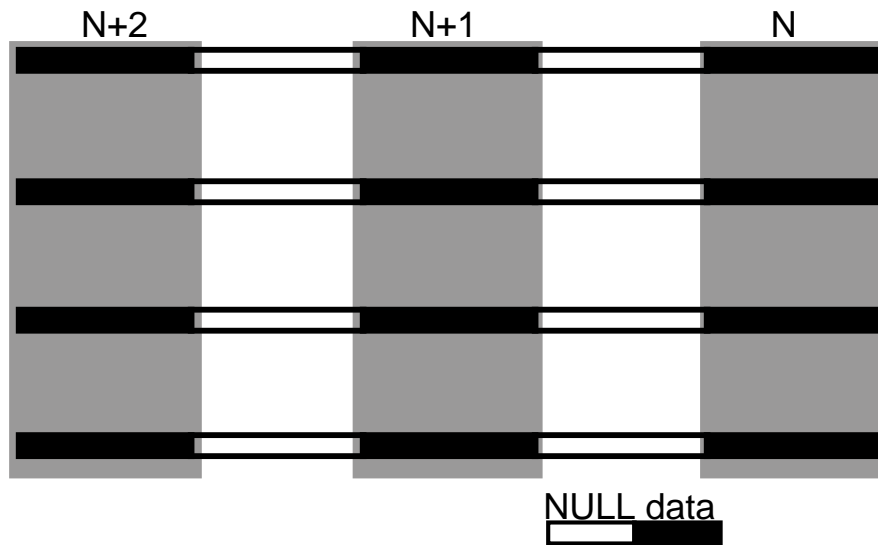
2D pipelined data path with orthogonal steering variable pipelines and triangle buffer



top down view of 3 way fan out

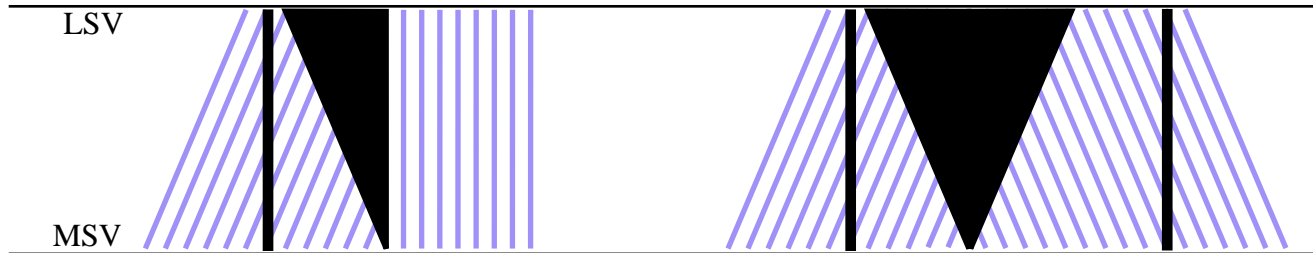


The Throughput Effect of 2D Pipelining



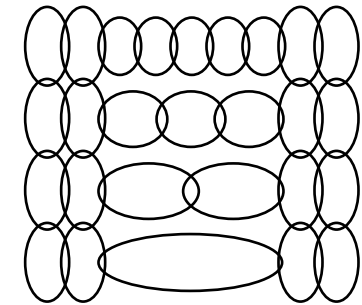
2D Triangle Buffering

The wavefronts will flow at a slope determined by the relative throughputs of the orthogonal pipelines. The slope can be changed with triangle buffers to match functions that require specific slopes such as clocked interfaces or barrel shifters.



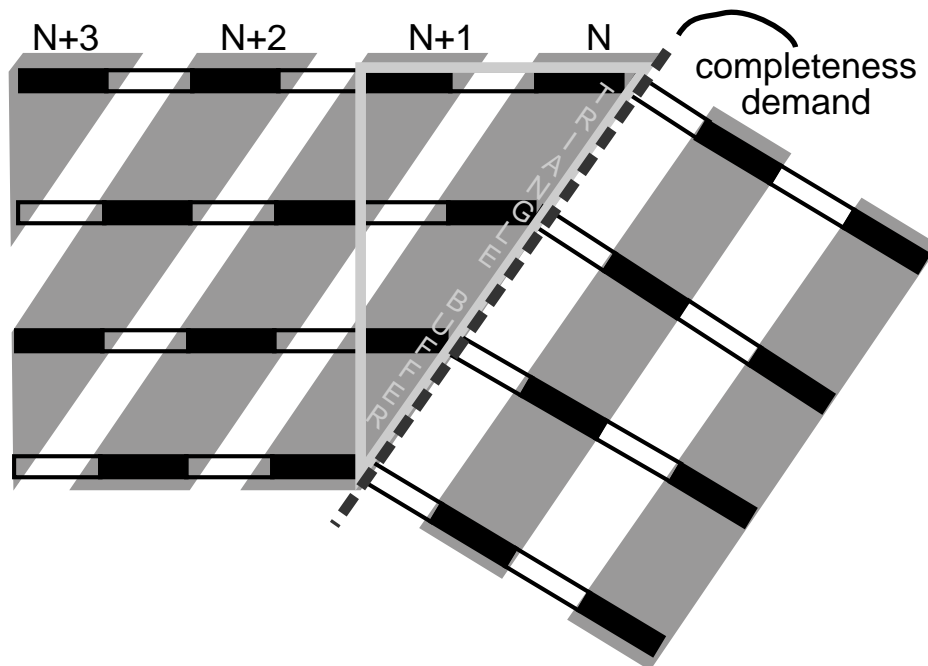
a. Positive slope to vertical slope

b. Positive slope to negative slope

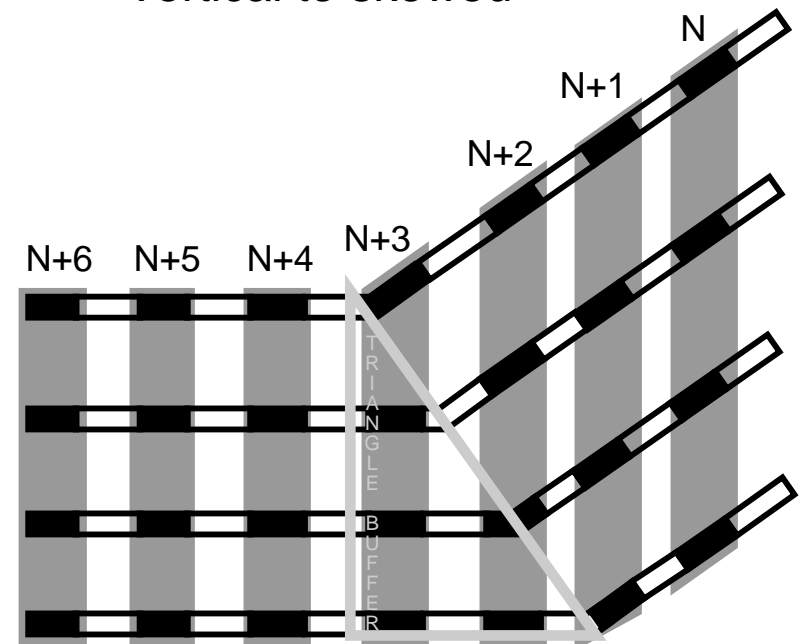


c. cycle structure of triangle buffer

Skewed to vertical



Vertical to skewed



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