Presentation Slides

Chapter 10

The Shadow Model of Pipeline Behavior

Logically Determined Design:

Clockless System Design With NULL Convention Logic

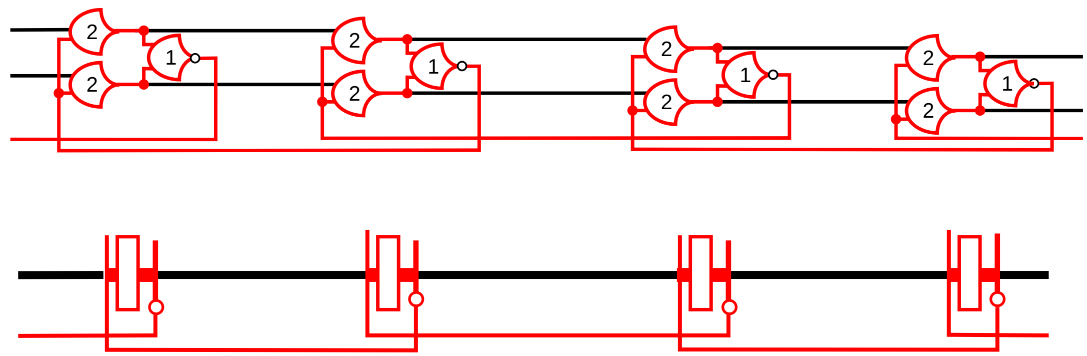
by Karl Fant

John Wiley & Sons, Inc.

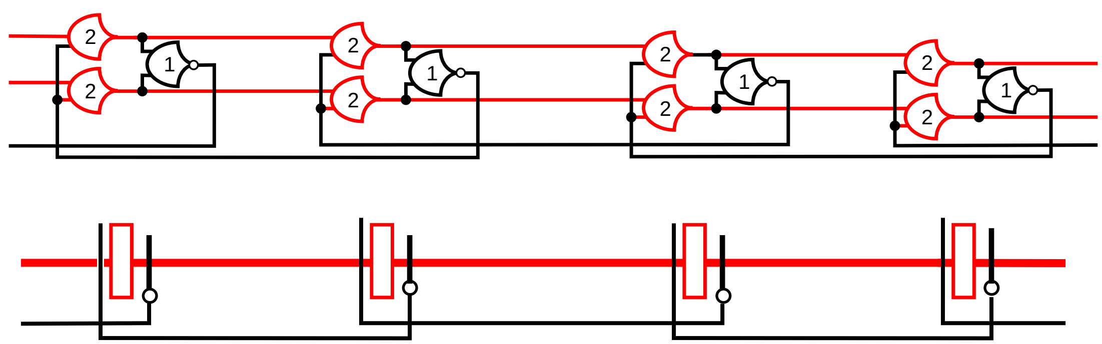
Presents an intuitive model of wavefront behavior in a logically determined pipeline.

Pipeline structures

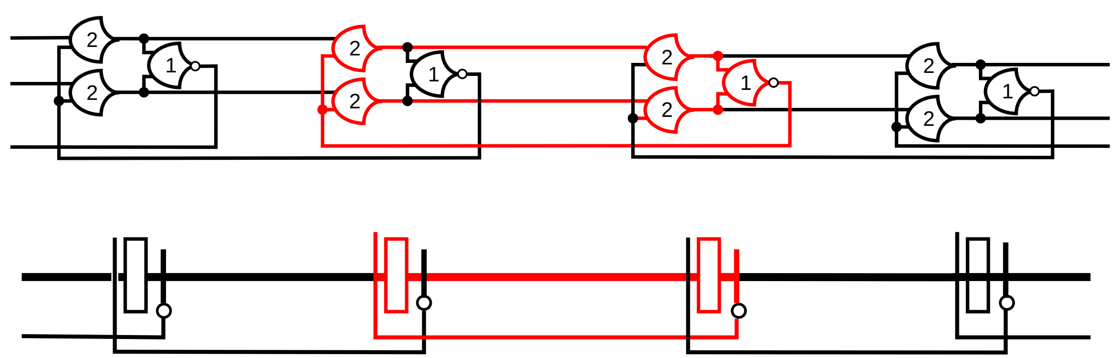
Bubble path
Acknowledge path,
reverse latency



Wavefront path
Data path,
forward latency



Cycle path



Wavefronts and Bubbles

DATA bubble

DATA in a CYCLE enabled for NULL is a DATA bubble and a NULL wavefront can overwrite it.

DATA wavefront

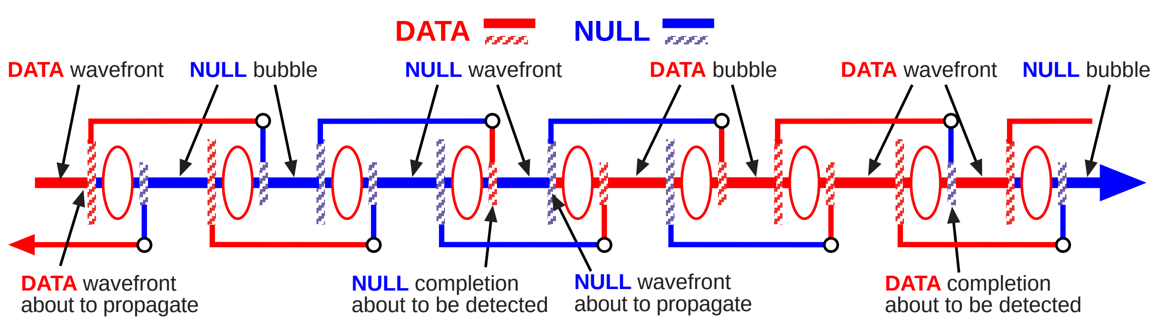
DATA in a cycle enabled for DATA is a DATA wavefront. It is stably maintained and a NULL wavefront cannot overwrite it.

NULL bubble

A NULL signal in a stage with a request for DATA is a NULL bubble and a DATA wavefront can overwrite it.

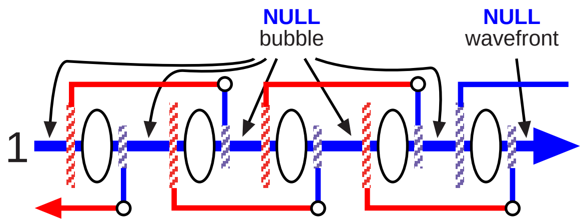
NULL wavefront

NULL in a cycle enabled for NULL is a NULL wavefront. It is stably maintained and a DATA wavefront cannot overwrite it.

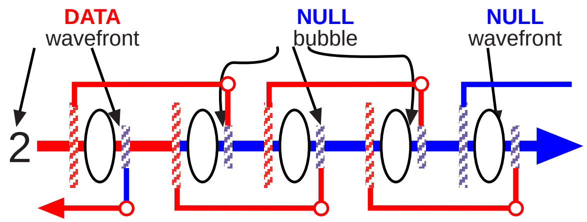


Wavefront Behavior 1

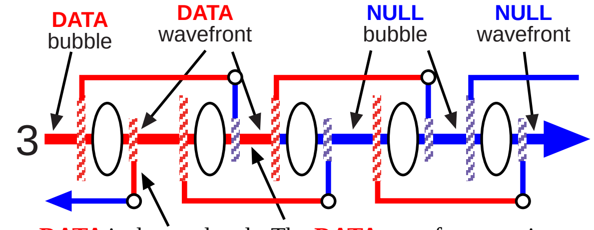
DATA **NULL**



The pipeline is occupied by a five cycle **NULL** bubble awaiting the arrival of a **DATA** wavefront.

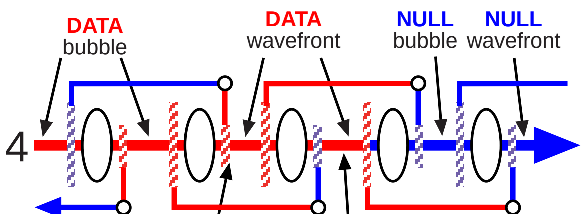


A **DATA** wavefront arrives and begins flowing through the **NULL** bubble.



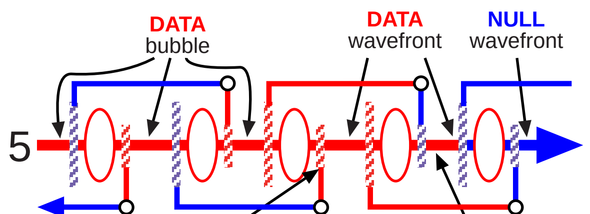
DATA is detected and **NULL** is requested.

The **DATA** wavefront continues to flow through the **NULL** bubble.



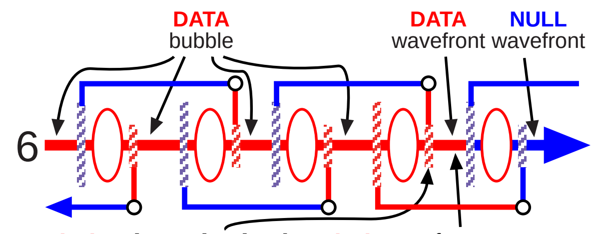
DATA is detected and **NULL** is requested.

The **DATA** wavefront continues to flow through the **NULL** bubble.



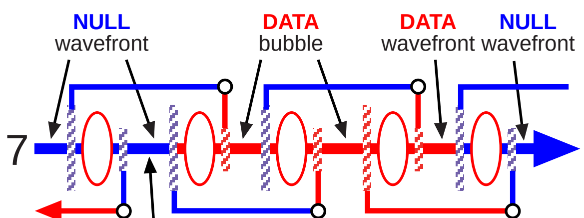
DATA is detected and **NULL** is requested.

The **DATA** wavefront continues to flow through the **NULL** bubble.

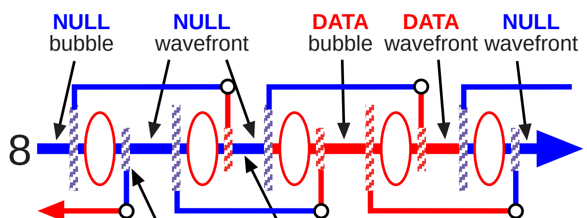


DATA is detected and **NULL** is requested.

The **DATA** wavefront is now blocked and will not overwrite the **NULL** wavefront.

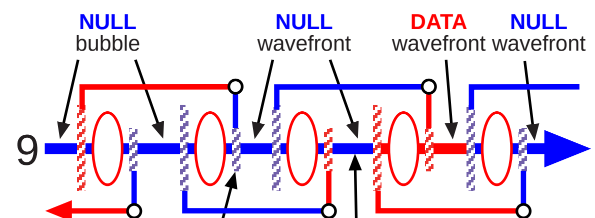


A **NULL** wavefront arrives and begins flowing through the **DATA** bubble.



NULL is detected and **DATA** is requested.

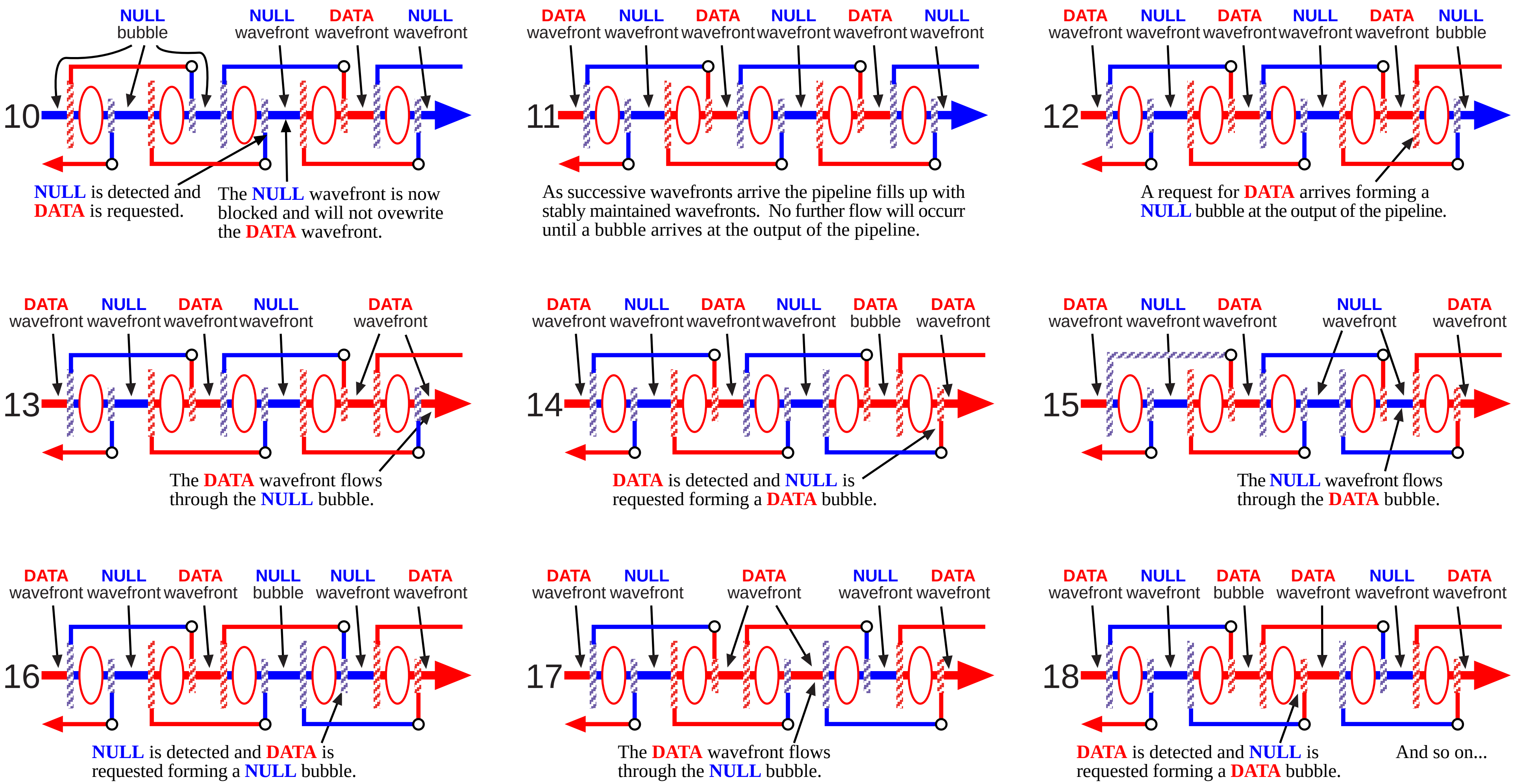
The **NULL** wavefront continues to flow through the **DATA** bubble.



NULL is detected and **DATA** is requested.

The **NULL** wavefront continues to flow through the **DATA** bubble.

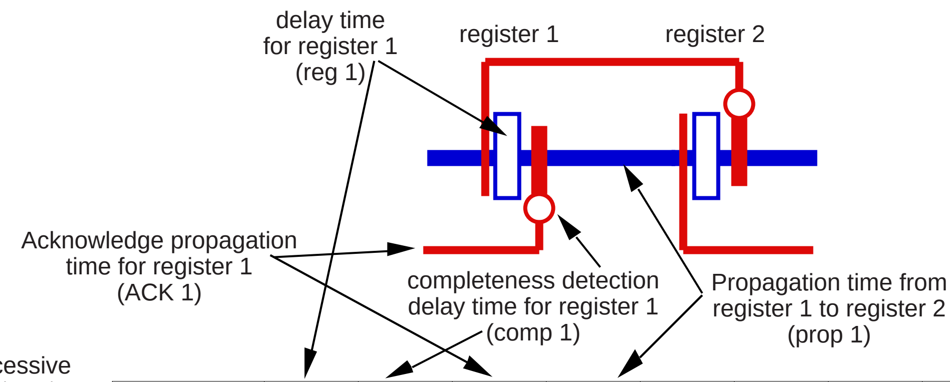
Wavefront Behavior 2



Wavefronts flow forward through bubbles.
Bubbles flow backward around wavefronts.
This spontaneous counterflow of wavefronts and bubbles
provides the dynamic behavior of logically determined pipelines.

Excel Pipeline simulation

The diagrams in this presentation are generated by a pipeline simulation implemented as an Excel spreadsheet

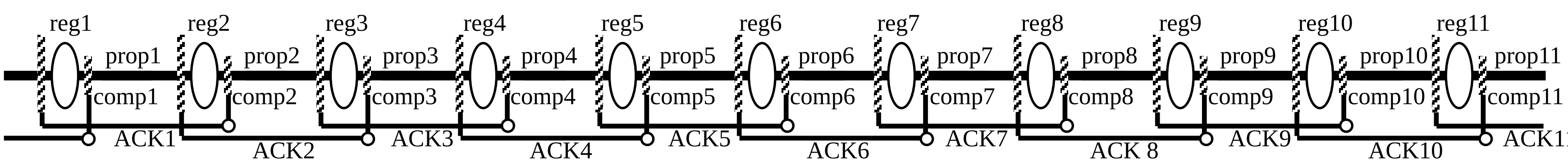


Successive register stages

Successive wavefronts

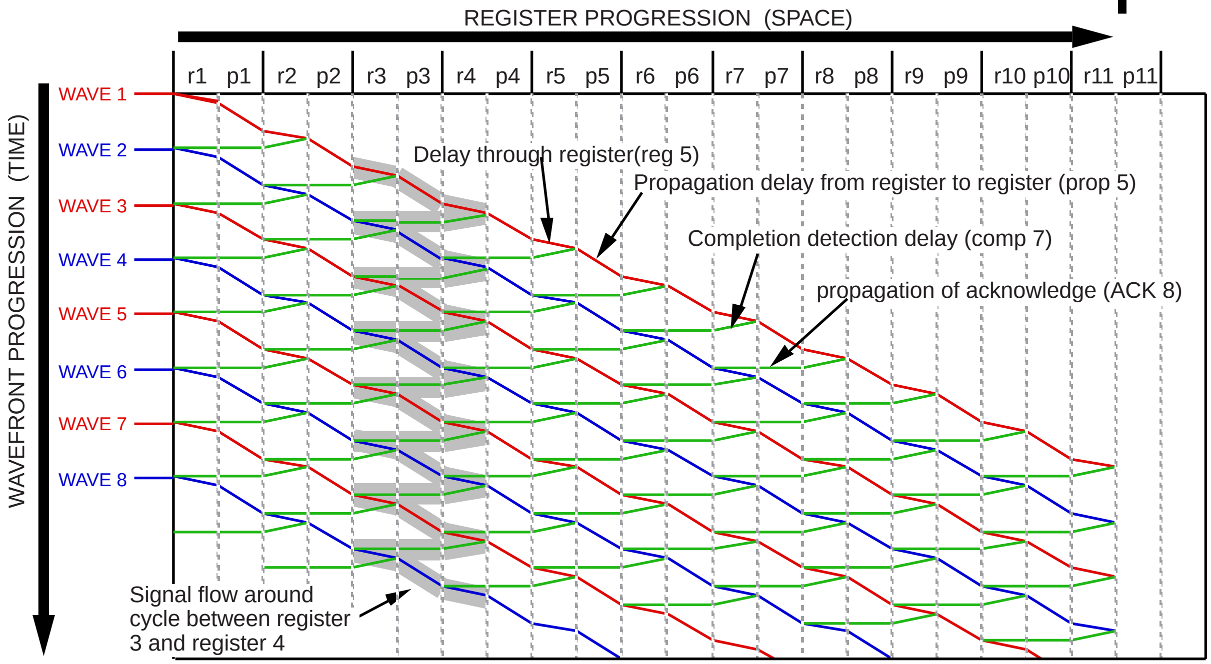
	reg 1	comp 1	ACK 1	prop1	reg 2	comp 2	ACK 2	prop2	reg 3
WAVE 1	1	1	0	3	1	1	0	3	1
WAVE 2	1	1	0	3	1	1	0	3	1
WAVE 3	1	1	0	3	1	1	0	3	1
WAVE 4	1	1	0	3	1	1	0	3	1
WAVE 5	1	1	0	3	1	1	0	3	1
WAVE 6	1	1	0	3	1	1	0	3	1
WAVE 7	1	1	0	3	1	1	0	3	1
WAVE 8	1	1	0	3	1	1	0	3	1

Simulation setup table

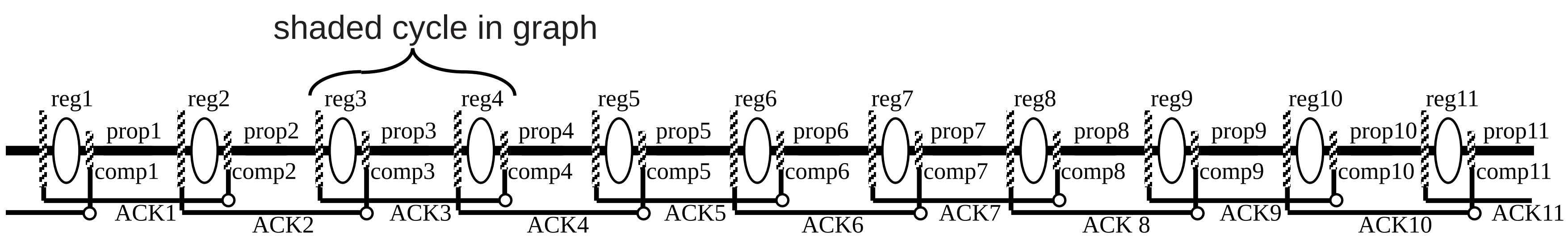


Pipeline modeled by simulation

Baseline Simulation Graph



Baseline graph of pipeline behavior
In this graph the corresponding delays of all cycles are equal and constant.

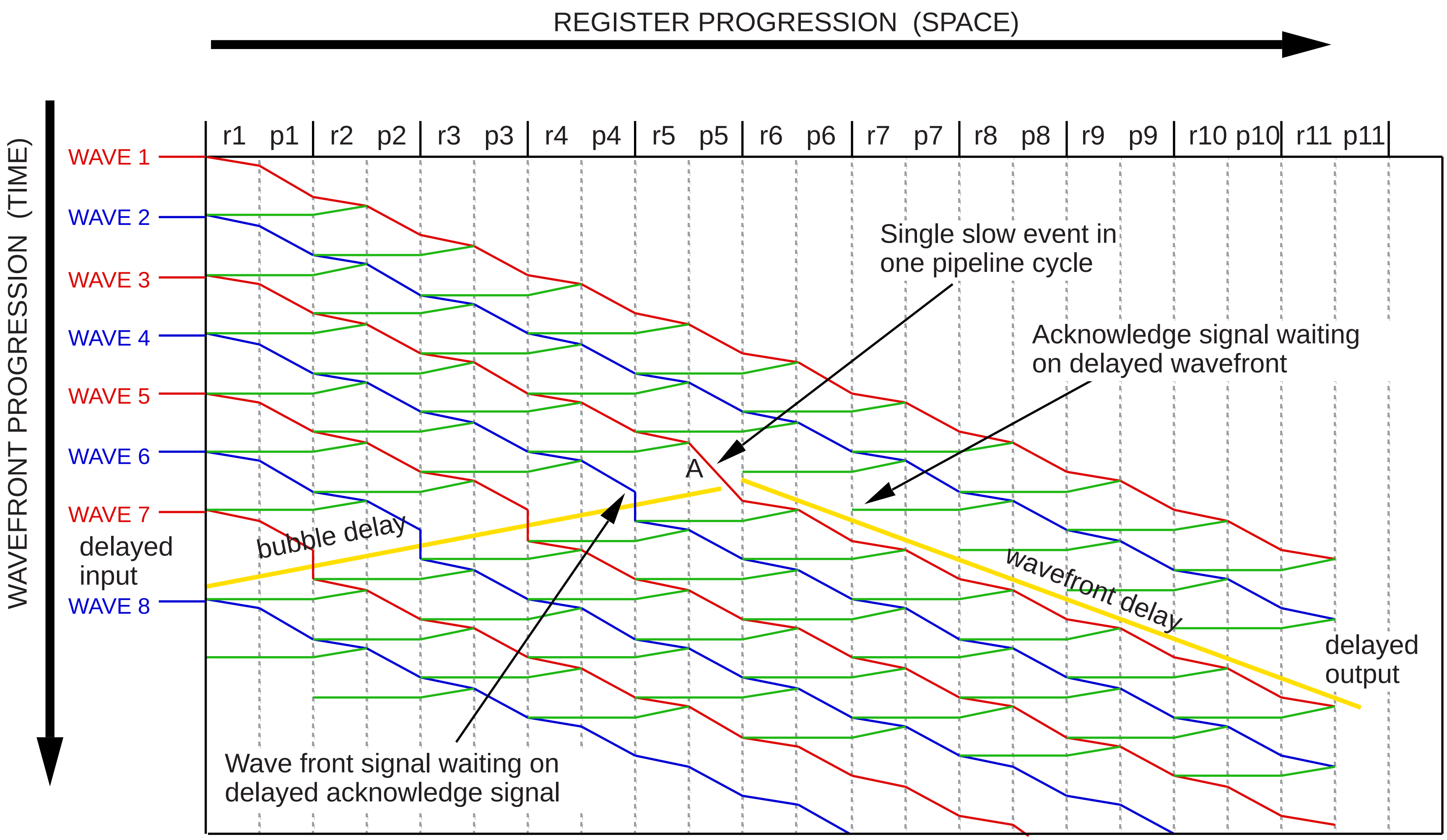


Pipeline Throughput

The throughput of a logically determined pipeline is the wavefronts propagating through a cycle of the pipeline per time interval. The DATA throughput is 1/2 the wavefront throughput.

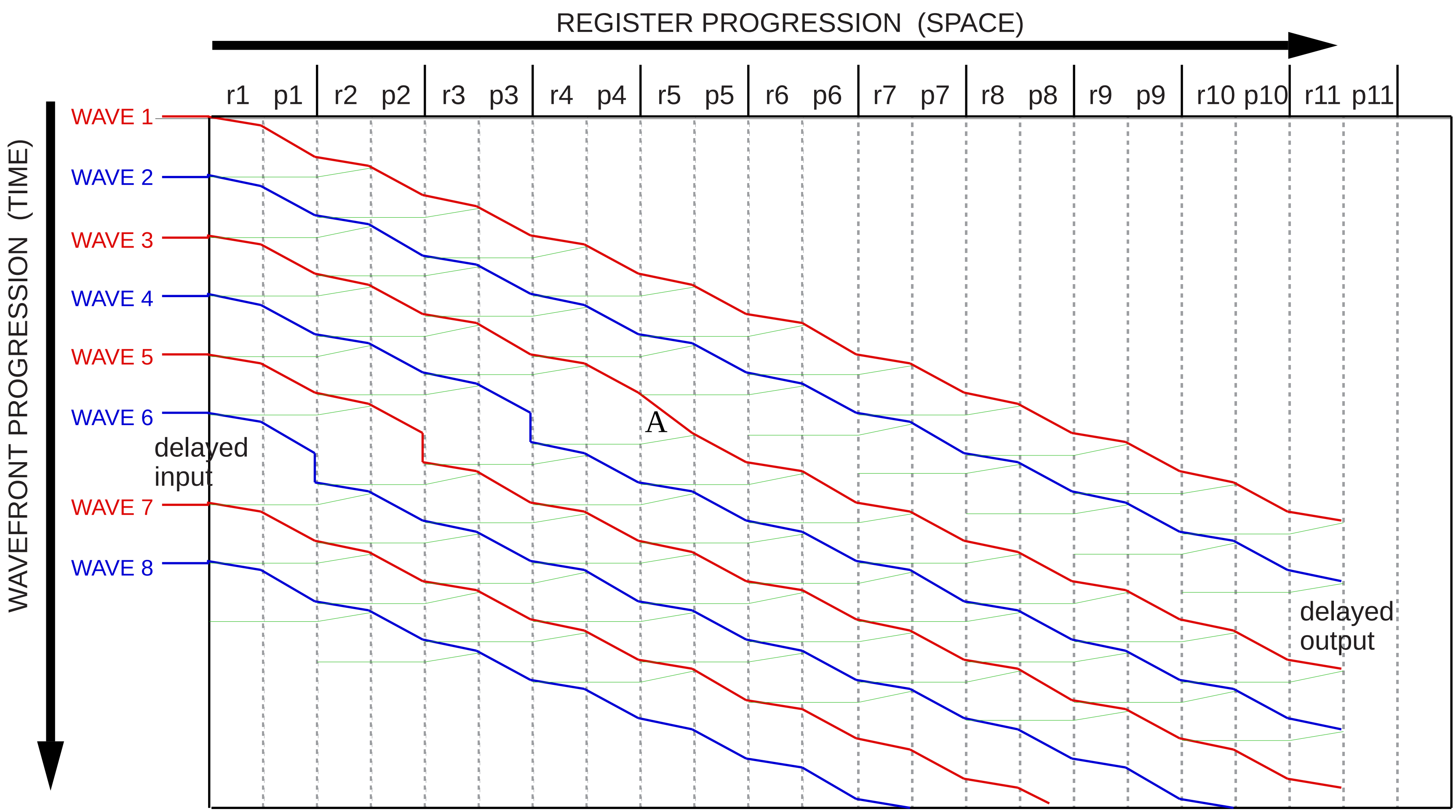
The throughput can be observed by viewing transitions on any path of the pipeline

Single Slow Delay Event: Prop5



The delay event propagates a delay along the bubble path causing wavefronts to wait and propagates a delay along the wavefront path causing bubbles to wait. These delays propagate to the input and the output of the pipeline causing input and output wavefronts to be delayed in time reducing the throughput of the pipeline.

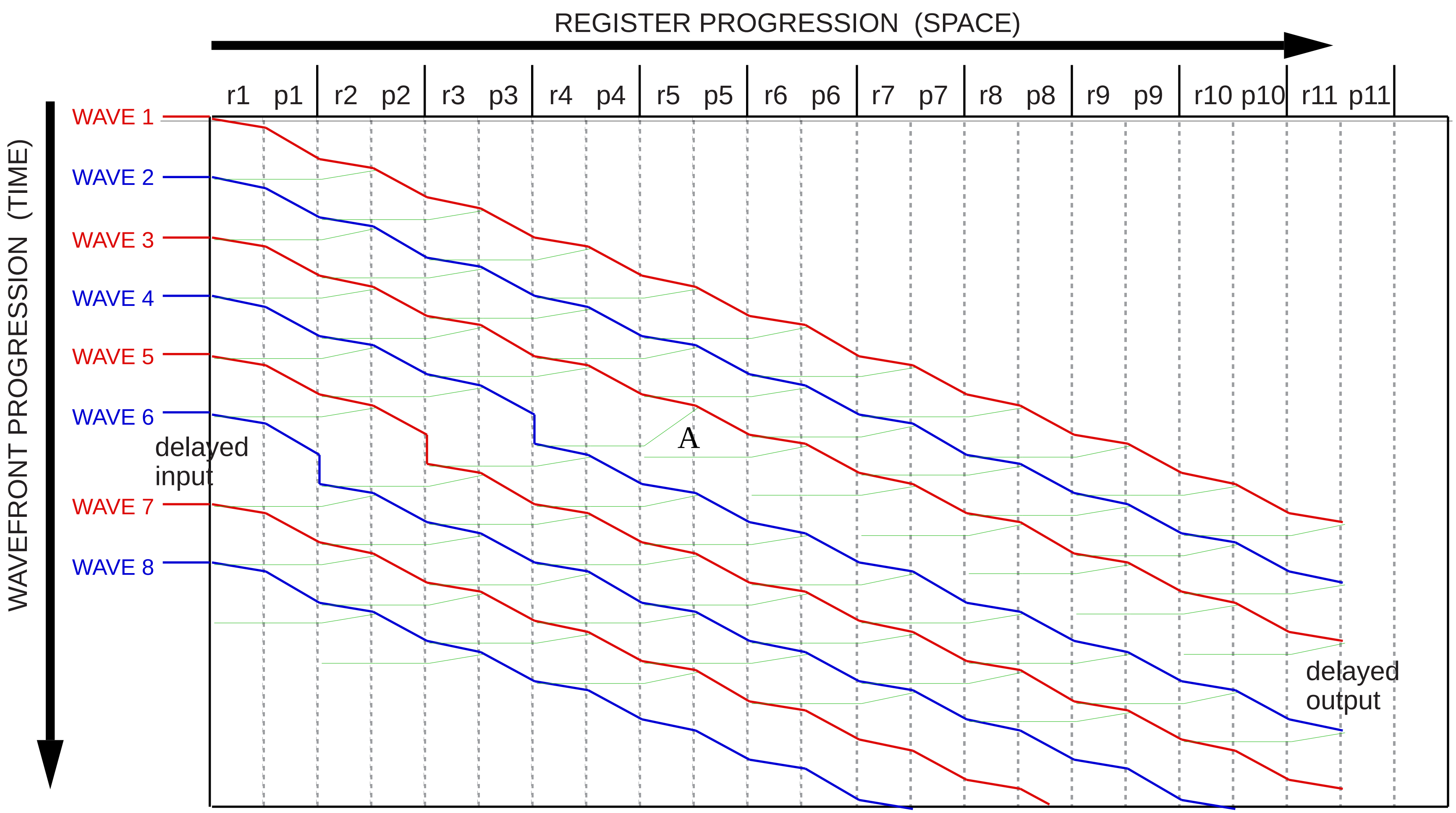
Delay in Register Path: Reg5



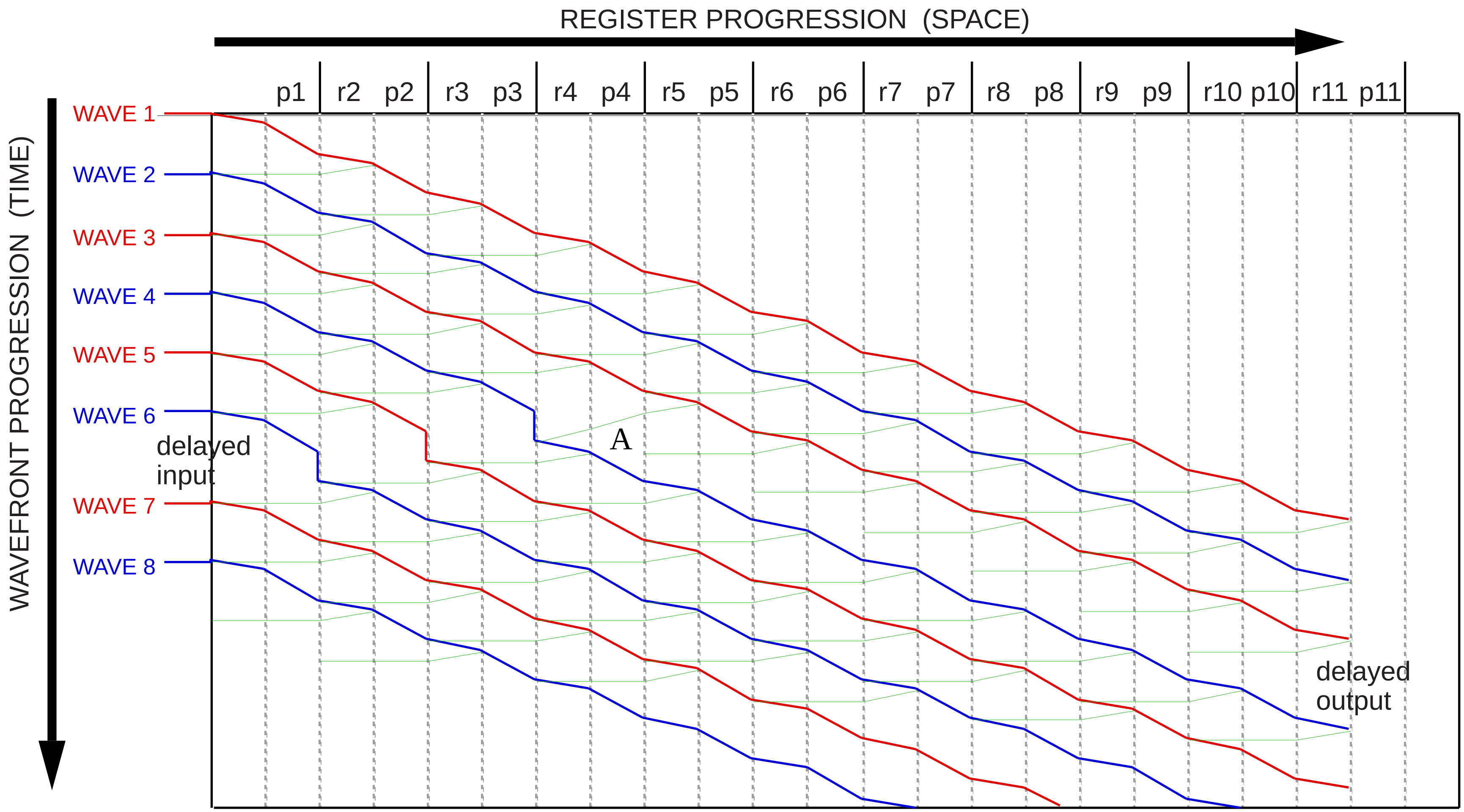
It does not matter where in a cycle a delay occurs. **The critical factor is the cycle period**. The previous slide, this slide and the next two slides show identical delays in different paths of the cycle. Each delay causes an identical compromise to the throughput.

Previous slide:	delay in propagation path.	This slide:	delay in register path.
Next slide:	delay in completeness path.	Next+1 slide:	delay in Acknowledge path.

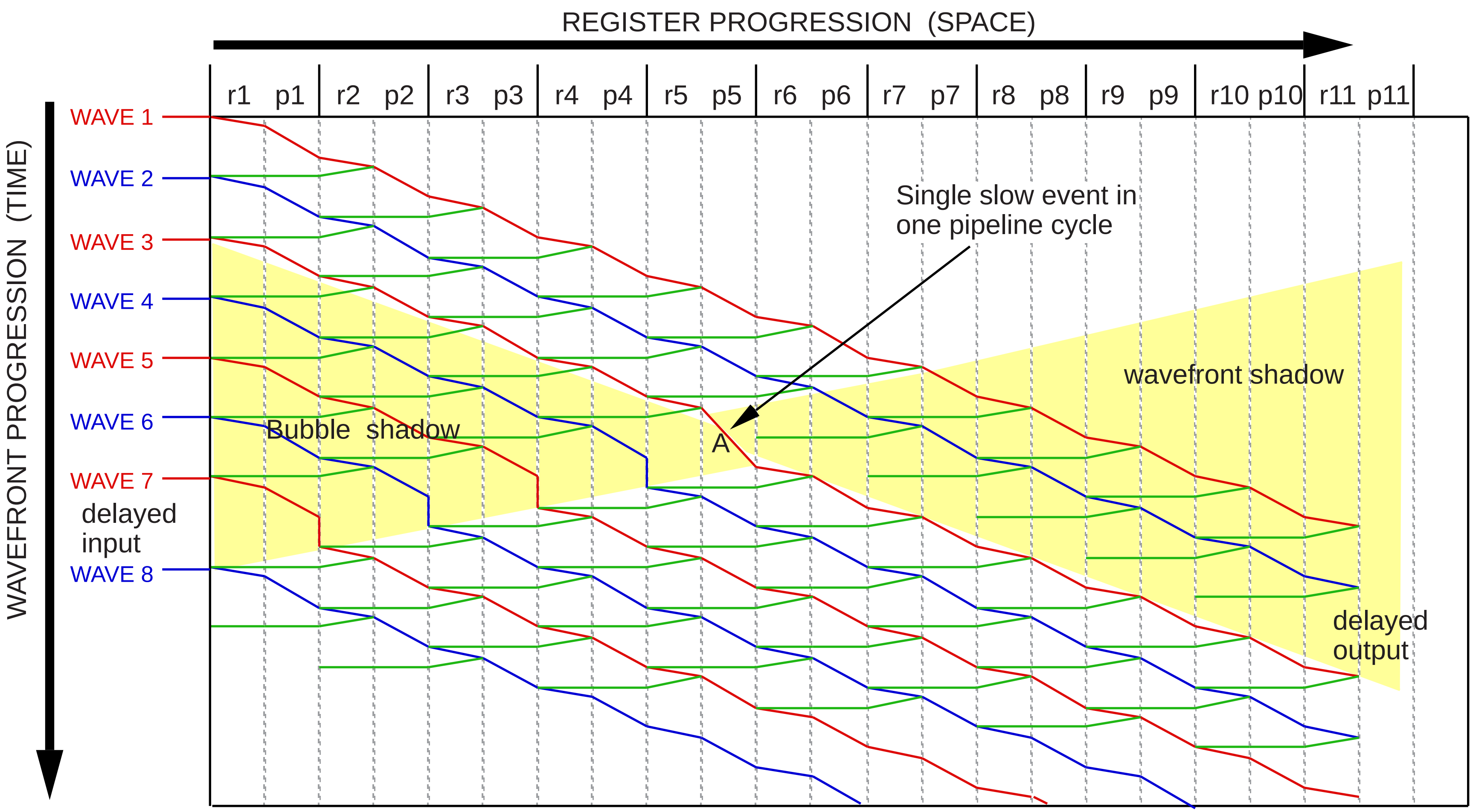
Delay in Completeness Path: Comp5



Delay in Acknowledge Path: Ack5

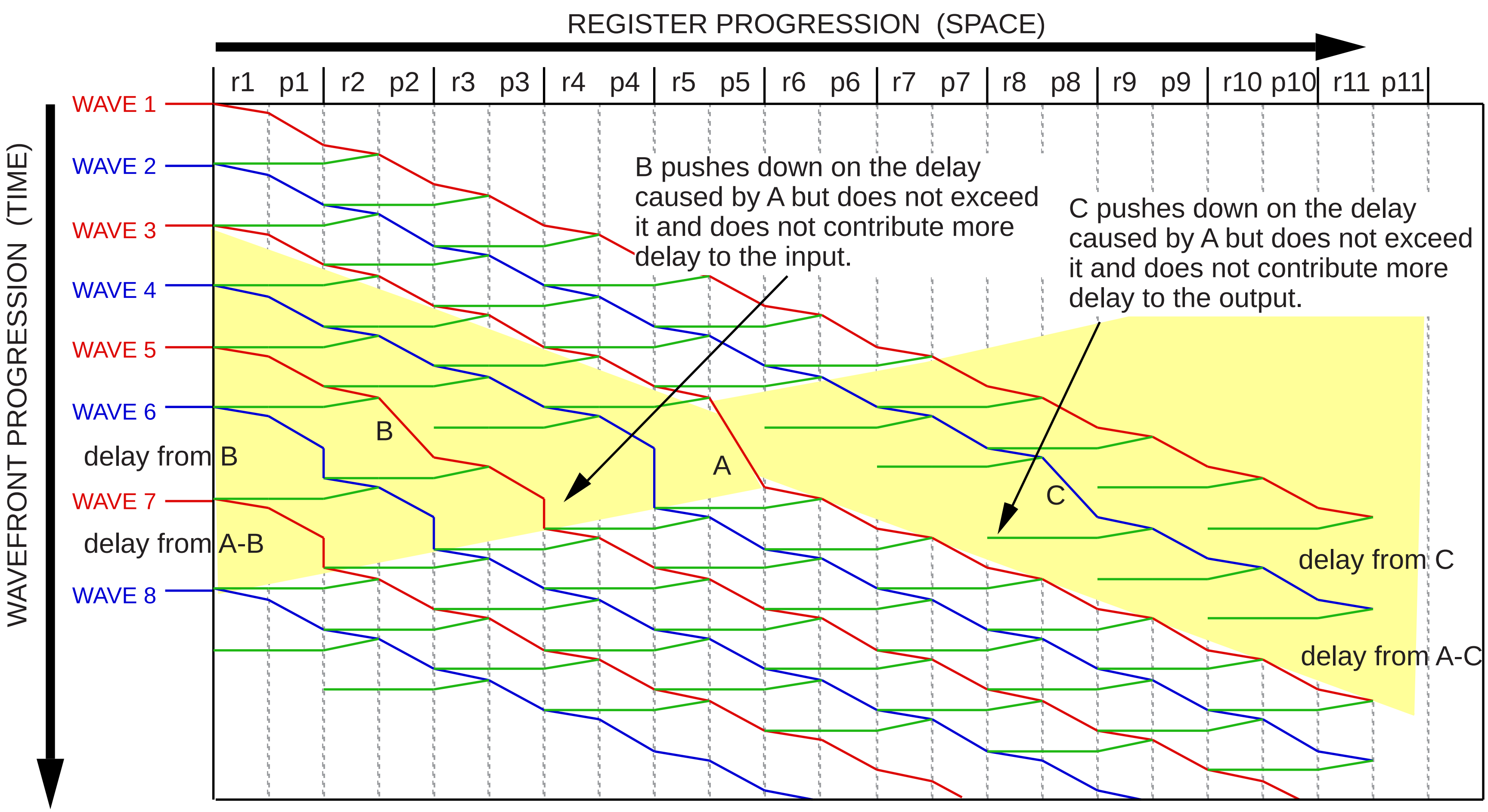


The Influence Shadow of the Delay



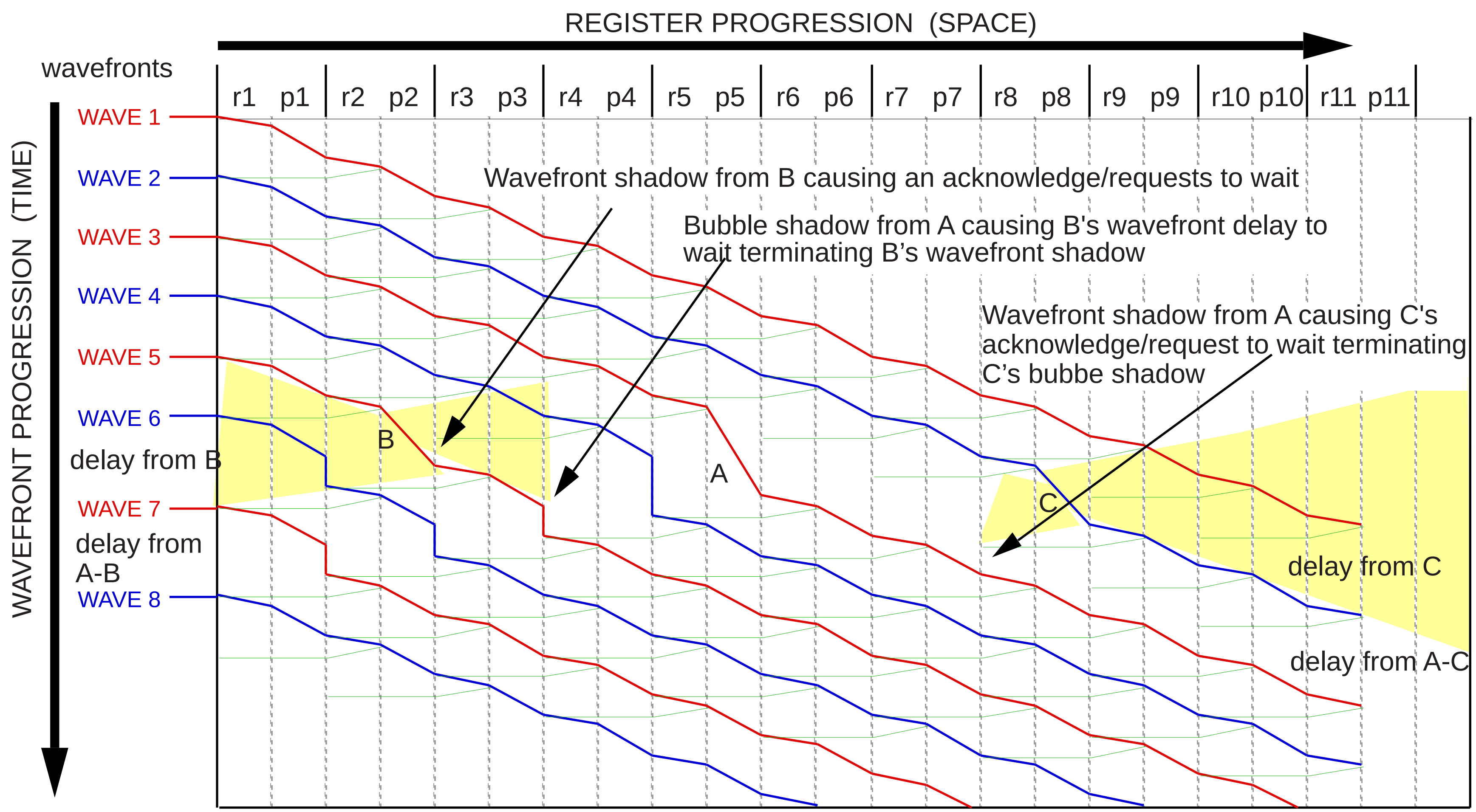
The delay event projects a shadow of influence over other wavefronts propagating through the pipeline. **A shorter delay within the shadow of a larger delay will have no effect on the throughput of the pipeline**. The shorter delay is said to be shadowed by the larger delay.

Long Delays Shadow Short Delays



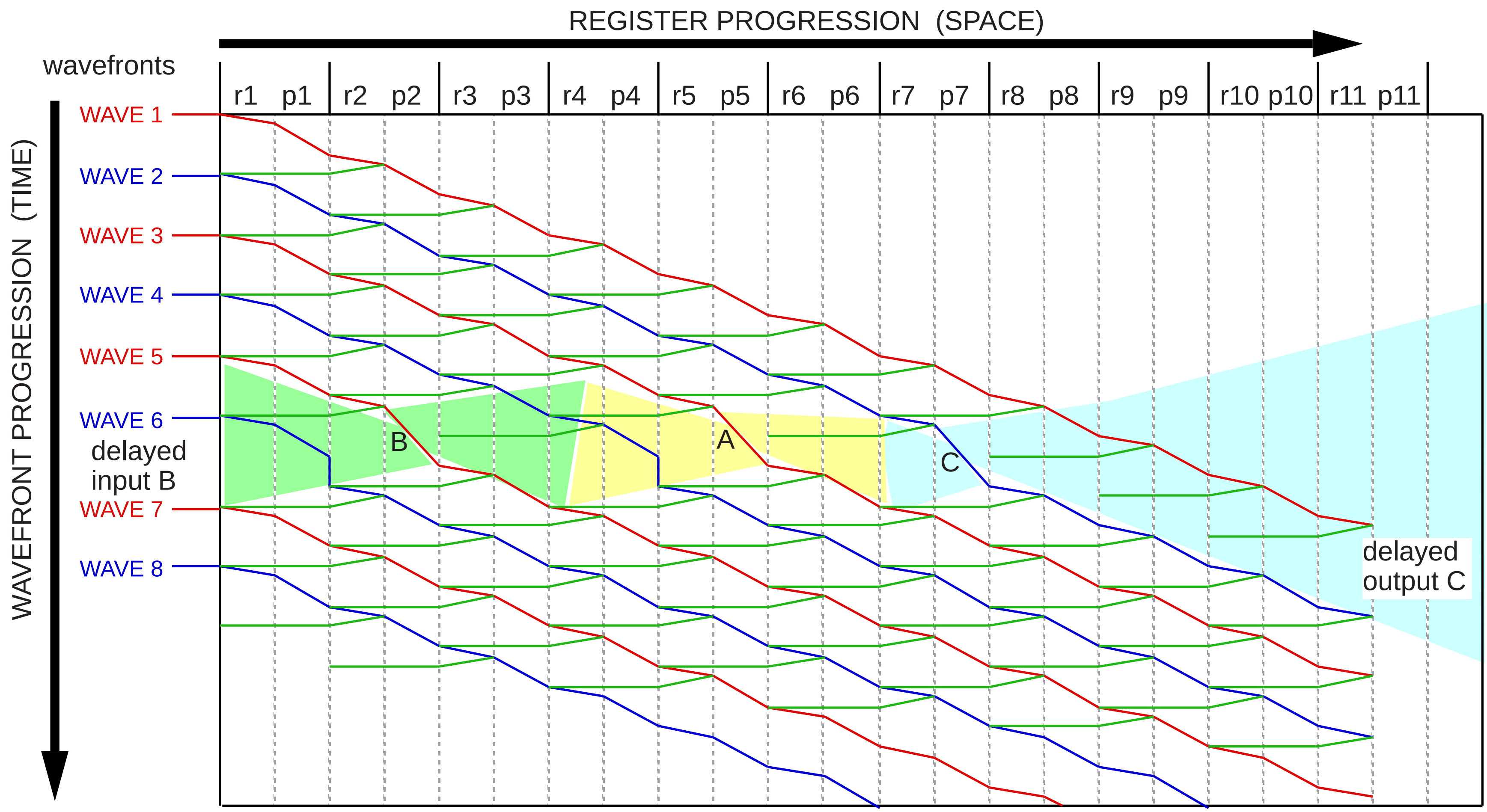
The delay of A shadows the delays of both B and C. While the B and C delays redistribute the delay affect of A at the input and output they do not increase or decrease the total delay at the input and output and have no effect on the throughput of the pipeline. The effect on the throughput is entirely due to the delay of A.

The shadows of B and C



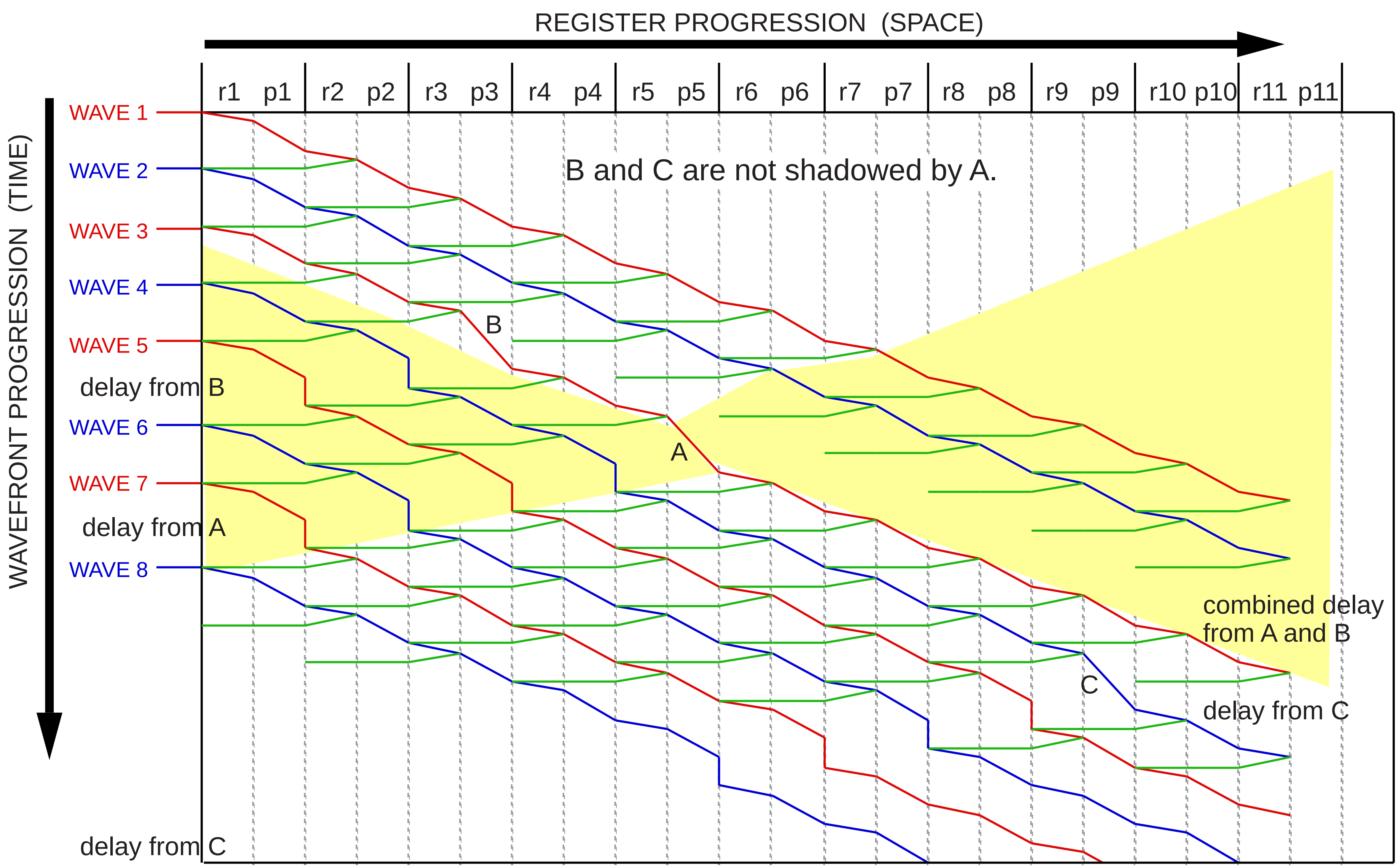
A delay projects a shadow as long as it propagates a wait. If the propagated wait is itself caused to wait its projected shadow is terminated.

Mutually Shadowing Equal Delays



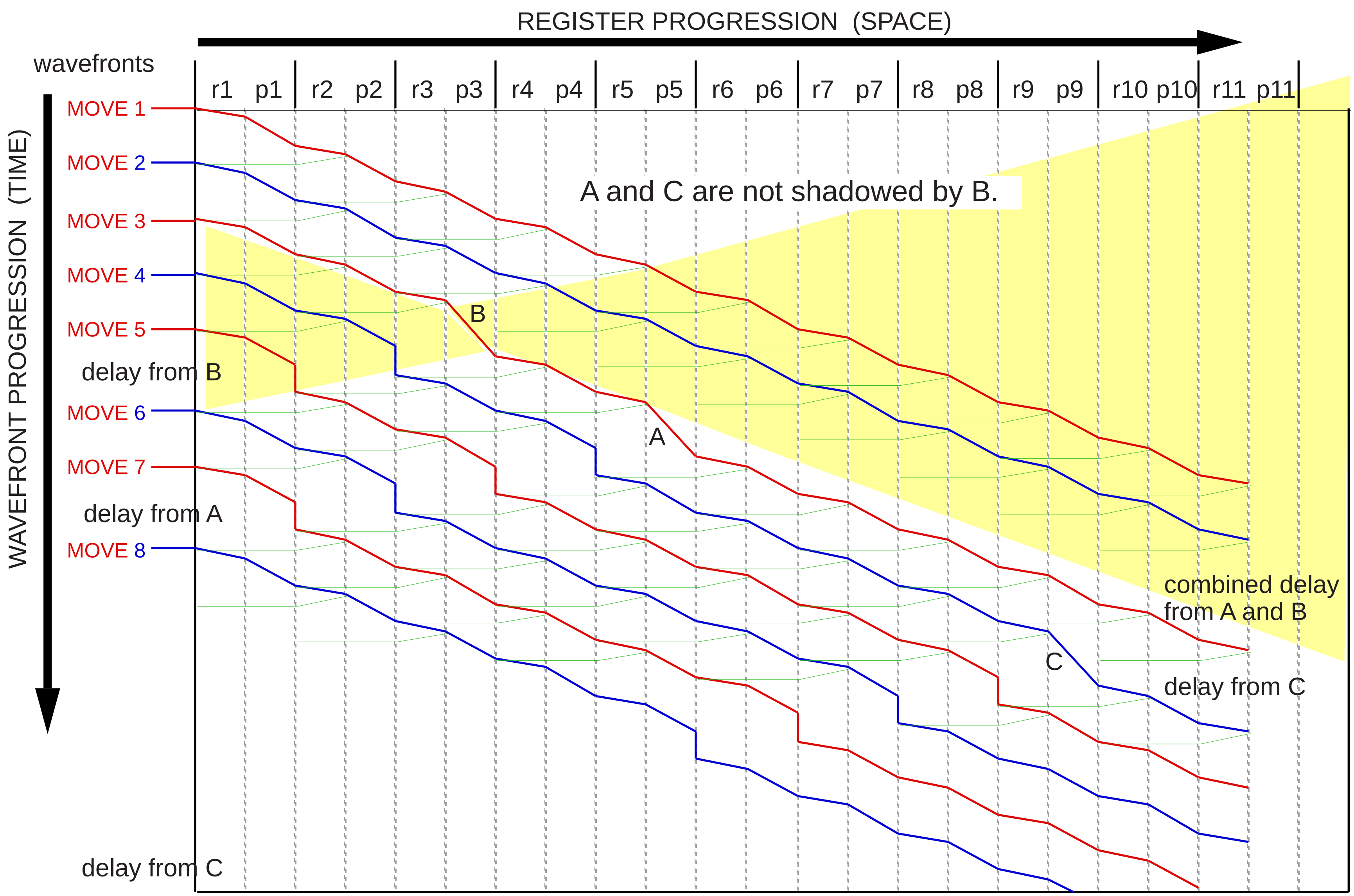
If equal delays mutually shadow each other **the effect on the throughput is as if there was only one delay**. Delays A and C are shadowed from the input by delay B and delays A and B are shadowed from the output by delay C.

Non-Shadowing Equal Delays



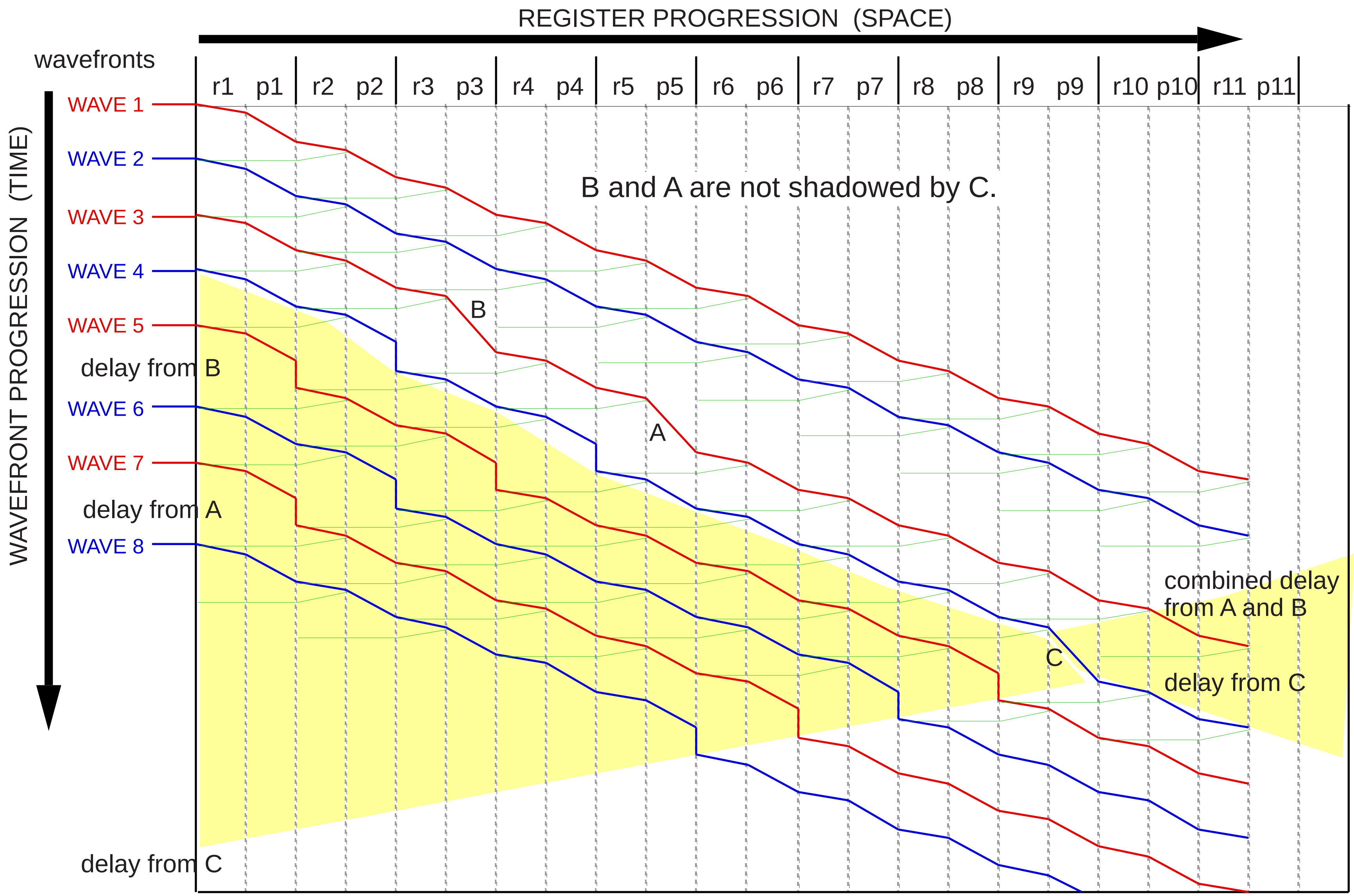
Delays A, B and C do not shadow each other and all three delays affect the throughput of the pipeline. Delay A does not shadow B or C.

Delay B Shadow



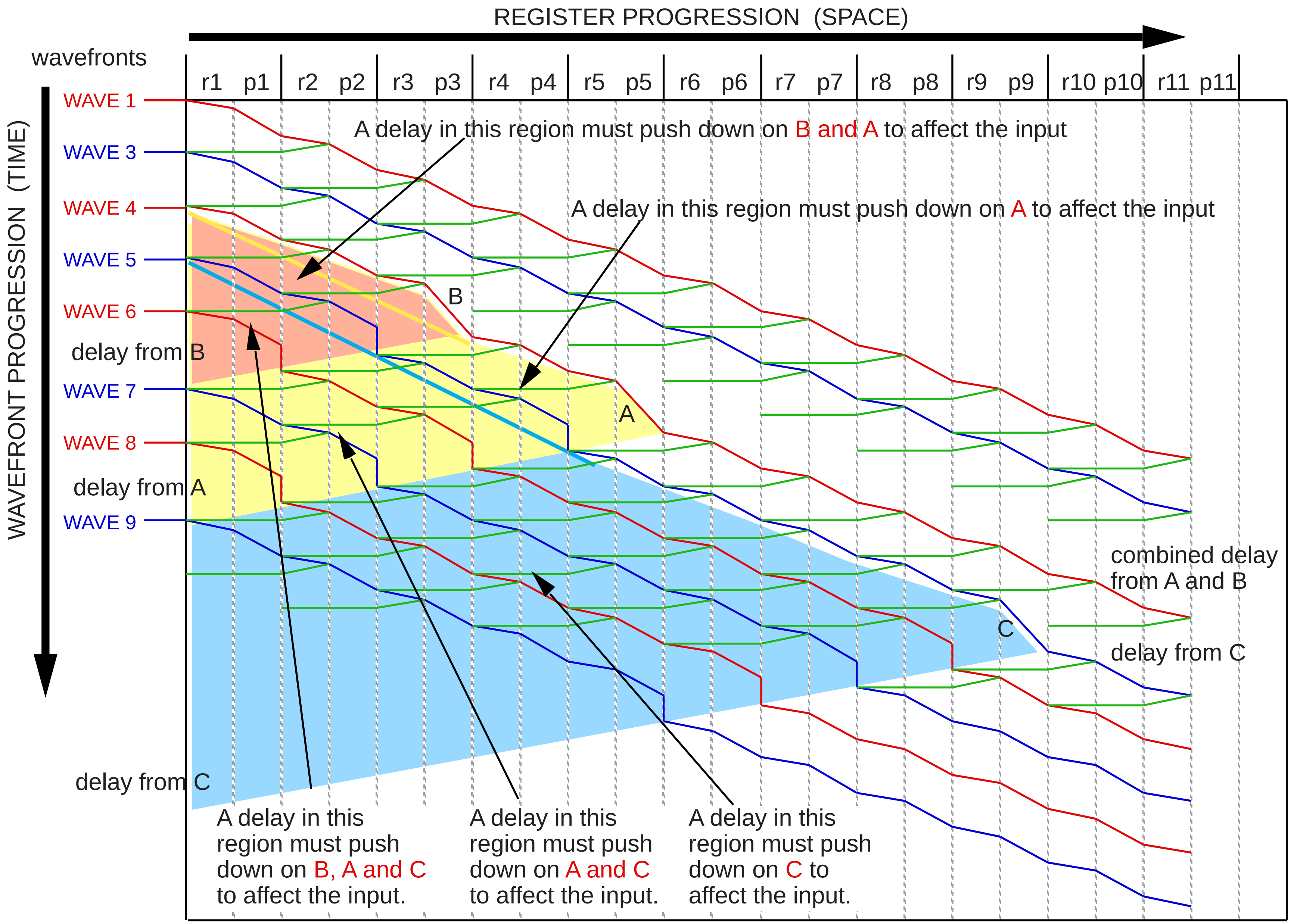
Delay B does not shadow A or C.

Delay C Shadow

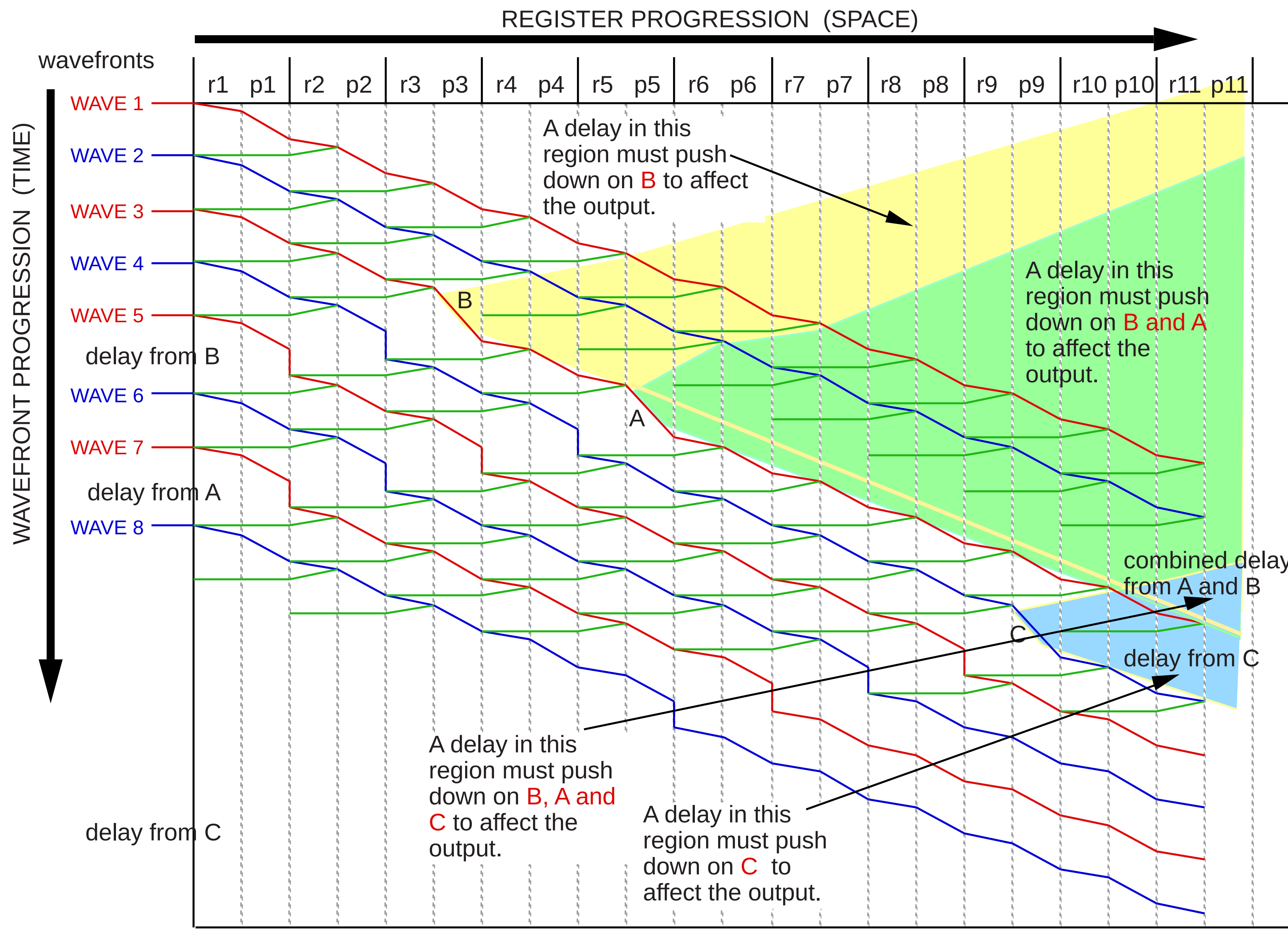


Delay C does not shadow B or A.

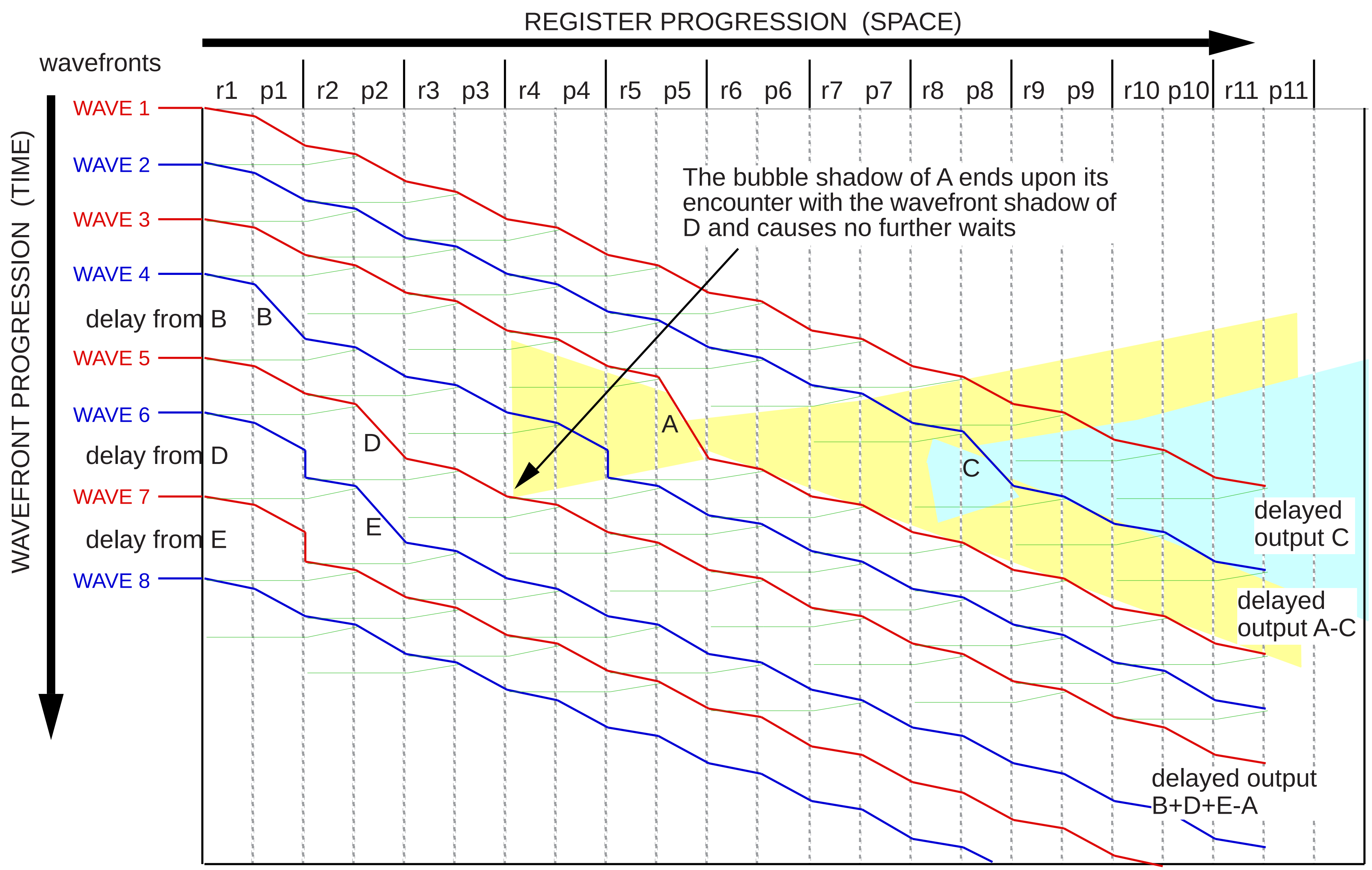
Additive Interaction of Intersecting Bubble Shadows



Additive Interaction of Intersecting Wavefront Shadows



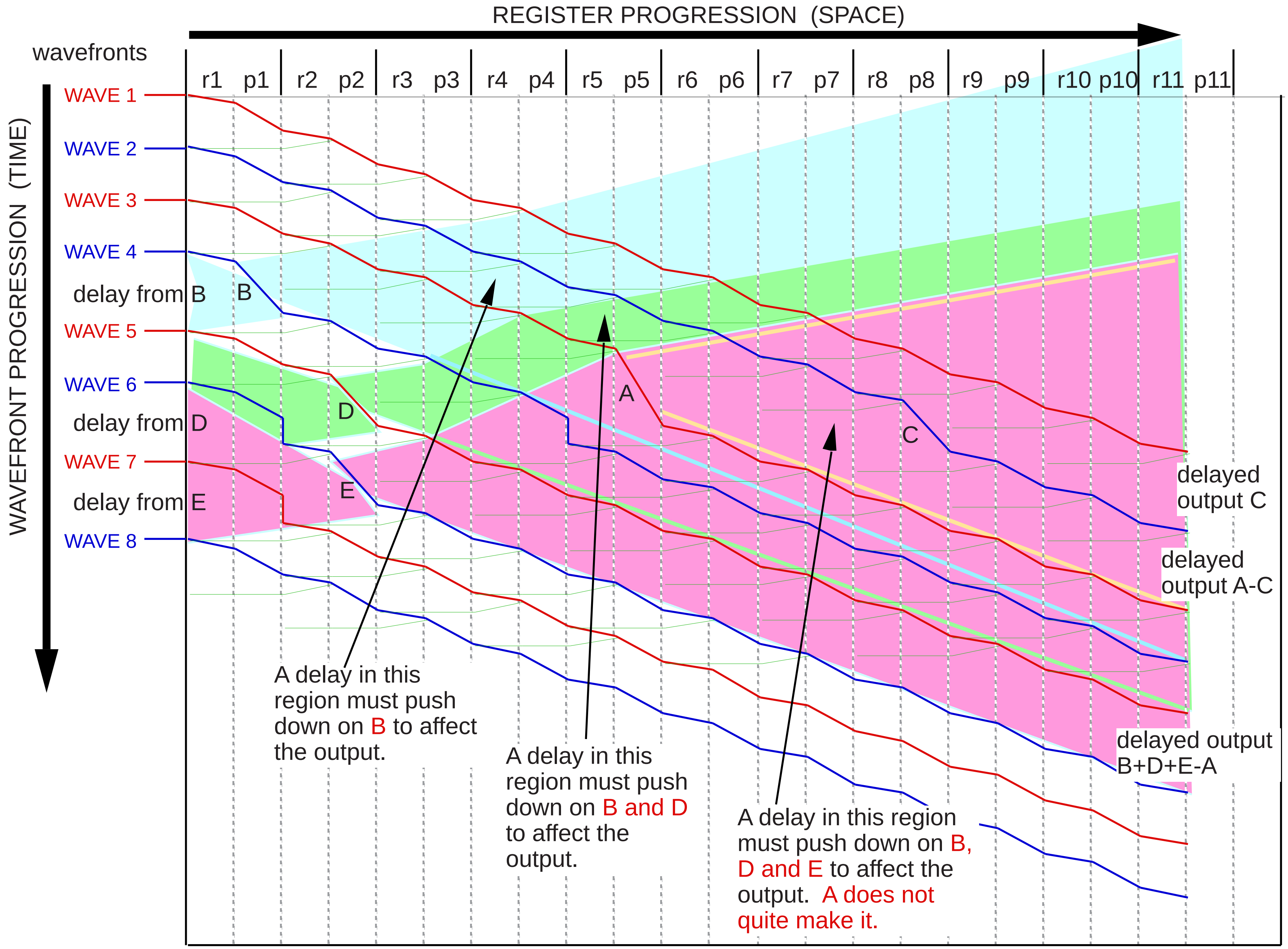
Short Delays can Accumulate to Shadow a Longer Delay



Shorter delays, that do not shadow each other, inside the shadow of a longer delay can accumulate and break out of the shadow of the longer delay and affect the throughput.

B and D accumulate to shadow A

Short Delays Accumulate to Shadow a Longer Delay



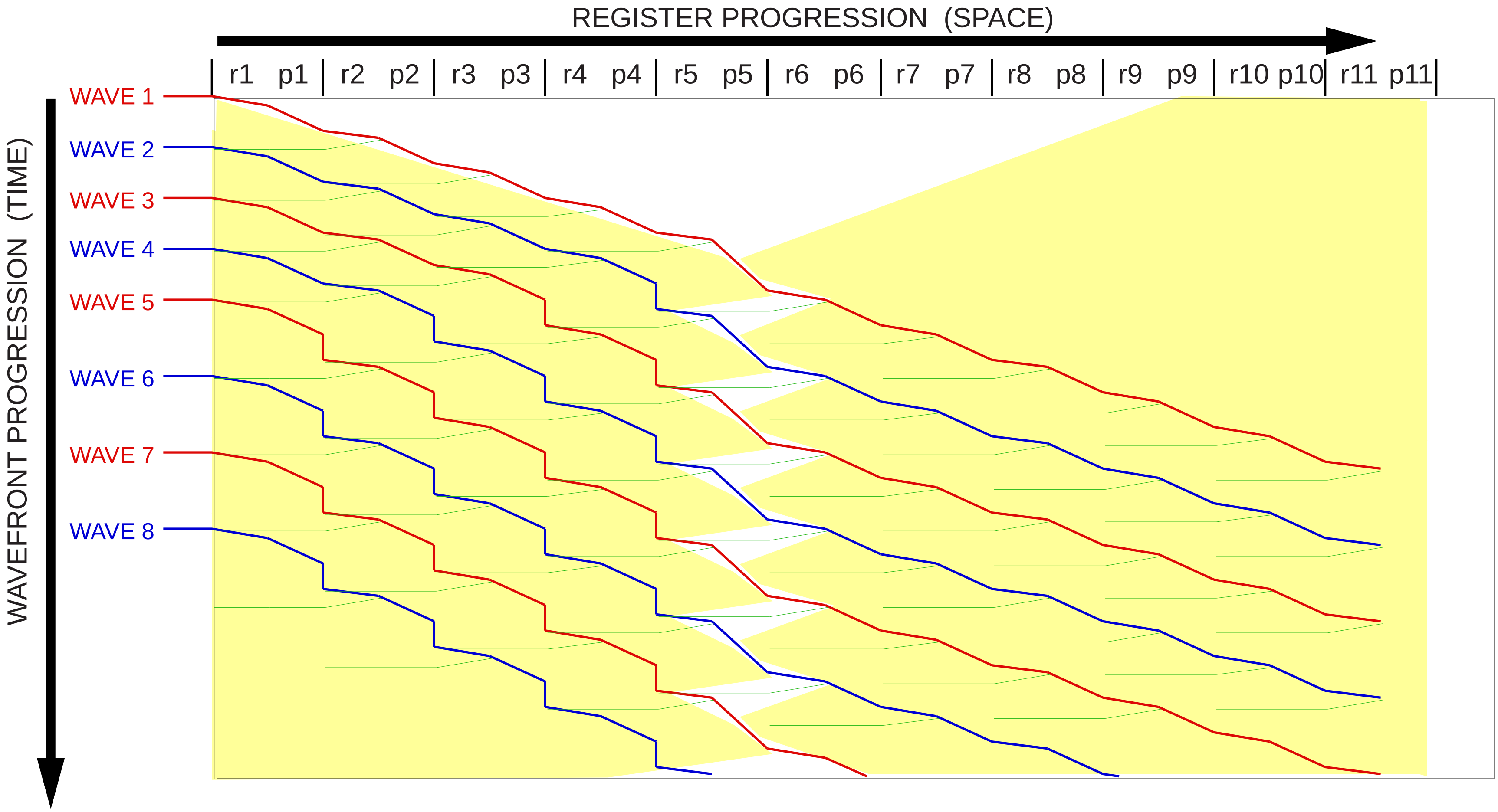
The Value of the Shadow Model

Pipeline behavior is typically considered too complex and dynamic for human intuition to deal with.

While shadow intersections can get quite complex, the shadow model allows one to eliminate a large amount of pipeline behavior as irrelevant to throughput, to focus on what is relevant and to characterize collective behavior intuitively with a clear understanding of the mechanism underlying the behavior.

Known observations about pipeline behavior can be understood directly in terms of the shadow model.

The Consistently Slow Cycle



A pipeline is only as fast as its slowest cycle. A single consistently slowest cycle will continually send successive shadows through the pipeline causing every other faster cycle in the pipeline to wait. **The throughput of the pipeline will be the throughput of that slowest cycle**. None of the faster cycles in the pipeline will affect the throughput of the pipeline.

Variable Cycle Periods

In a pipeline with cycles presenting a distribution of period behavior, every time any cycle has a long period the shadow of this long delay will project through the pipeline shadowing all shorter cycle periods in the pipeline

A slow cycle will almost always decrease the throughput of a pipeline and a fast cycle will almost never increase the throughput of a pipeline.

The behavior of the pipeline as a whole will tend towards worst case throughput of its individual cycles and will not deliver average case throughput of the cycle periods.

This page intentionally blank

This page intentionally blank